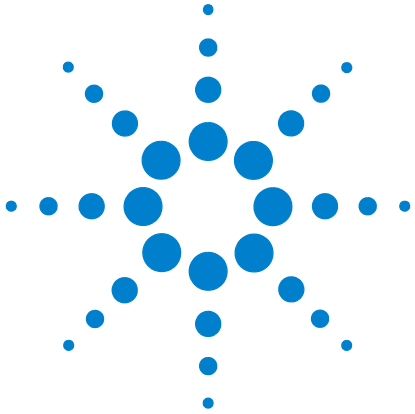

Agilent 16962A Logic Analyzer

Service Guide

Agilent Technologies

Notices

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Manual Part Number

16962-97000

Edition

First edition, May 2009

Available in electronic format only

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CAUTION

A **CAUTION** notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in damage to the product or loss of important data. Do not proceed beyond a **CAUTION** notice until the indicated conditions are fully understood and met.

WARNING

A WARNING notice denotes a hazard. It calls attention to an operating procedure, practice, or the like that, if not correctly performed or adhered to, could result in personal injury or death. Do not proceed beyond a WARNING notice until the indicated conditions are fully understood and met.

Additional Safety Notices

This apparatus has been designed and tested in accordance with IEC Publication 1010, Safety Requirements for Measuring Apparatus, and has been supplied in a safe condition. This is a Safety Class I instrument (provided with terminal for protective earthing). Before applying power, verify that the correct safety precautions are taken (see the following warnings). In addition, note the external markings on the instrument that are described under "Safety Symbols."

Warnings

- Before turning on the instrument, you must connect the protective earth terminal of the instrument to the protective conductor of the (mains) power cord. The mains plug shall only be inserted in a socket outlet provided with a protective earth contact. You must not negate the protective action by using an extension cord (power cable) without a protective conductor (grounding). Grounding one conductor of a two-conductor outlet is not sufficient protection.
- Only fuses with the required rated current, voltage, and specified type (normal blow, time delay, etc.) should be used. Do not use repaired fuses or short-circuited fuseholders. To do so could cause a shock or fire hazard.
- If you energize this instrument by an auto transformer (for voltage reduction or mains isolation), the common terminal must be connected to the earth terminal of the power source.
- Whenever it is likely that the ground protection is impaired, you must make the instrument inoperative and secure it against any unintended operation.
- Service instructions are for trained service personnel. To avoid dangerous electric shock, do not perform any service unless qualified to do so. Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.
- Do not install substitute parts or perform any unauthorized modification to the instrument.
- Capacitors inside the instrument may retain a charge even if the instrument is disconnected from its source of supply.
- Do not operate the instrument in the presence of flammable gasses or fumes. Operation of any electrical instrument in such an environment constitutes a definite safety hazard.
- Do not use the instrument in a manner not specified by the manufacturer.

To clean the instrument

If the instrument requires cleaning: (1) Remove power from the instrument. (2) Clean the external surfaces of the instrument with a soft cloth dampened with a mixture of mild detergent and water. (3) Make sure that the instrument is completely dry before reconnecting it to a power source.

Safety Symbols

Instruction manual symbol: the product is marked with this symbol when it is necessary for you to refer to the instruction manual in order to protect against damage to the product.

Hazardous voltage symbol.

Earth terminal symbol: Used to indicate a circuit common connected to grounded chassis.

Agilent 16962A Logic Analyzer—At a Glance

The 16962A logic analyzer module is for the 16901A or 16902B logic analysis system frames. It provides 2 GT/s state logic analysis and up to 8 GHz timing analysis. The 16962A has 4 M to 100 M sample memory depth (depending on the option chosen).

The 16962A logic analyzer module offers high performance measurement capability.

Features

Some of the main features of the 16962A are as follows:

- 68 data channels, including:
  - 2 clock/data channels.
  - 2 clock ready/data channels.
- 2 GT/s maximum state acquisition speed.
- “Eye scan” feature.
- 2 GHz timing analysis on all channels at full memory depth, 4 GHz timing analysis with 1/2 channels, and 8 GHz timing analysis with 1/4 channels.
- Expandable to 340 channels (5-card set).

Service Strategy

The service strategy for this instrument is the replacement of defective assemblies. This service guide contains information for finding a defective assembly by testing and servicing the 16962A logic analyzer module.

The modules can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

Contacting Agilent Technologies

To locate a sales or service office near you, go to www.agilent.com/find/contactus.

Application

This service guide applies to 16962A logic analyzer modules installed in 16901A or 16902B logic analysis system frames.

The 16962A Logic Analyzer

In This Service Guide

This book is the service guide for the 16962A logic analyzer module.

This service guide has eight chapters.

Chapter 1, “General Information” contains information about the module, lists accessories for the module, gives specifications and characteristics of the module, and provides a list of the equipment required for servicing the module.

Chapter 2, “Preparing for Use” tells how to prepare the module for use.

Chapter 3, “Testing Logic Analyzer Performance” gives instructions on how to verify that the module meets its specifications.

Chapter 4, “Calibrating” contains calibration instructions for the module (if required).

Chapter 5, “Troubleshooting” contains explanations of self-tests and flowcharts for troubleshooting the module.

Chapter 6, “Replacing Assemblies” explains how to replace the module and assemblies of the module and how to return them to Agilent Technologies.

Chapter 7, “Replaceable Parts” lists replaceable parts, shows an exploded view, and gives ordering information.

Chapter 8, “Theory of Operation” explains how the logic analyzer module works.

Contents

1 General Information

This chapter lists the accessories, some of the specifications and characteristics, and the recommended test equipment.

Accessories

One or more of the following accessories, sold separately, are required to operate the 16962A logic analyzer.

Probing Accessories

For information about probing accessories for logic analyzers with 90-pin pod connectors, see the *Probing Solutions for Logic Analyzers Catalog*, literature part number 5968-4632E, available on Agilent's web site (www.agilent.com).

Mainframe and Operating System

The 16962A logic analyzer requires a 16901A or 16902B logic analysis system frame. The 16962A logic analyzer requires software version 03.82 or higher.

Specifications

The specifications are the performance standards against which the product is tested.

16962A Logic Analyzer Specifications		
Parameter	**2 Gb/s mode**	**Notes**
Maximum state data rate	2 Gb/s	(DDR, 1 GHz clock), specified at probe tip.

Specifications verified under the following test conditions:		
Parameter	**2 Gb/s mode**	**Notes**
Vh	0.875 V	250 mV pp
Vl	0.375 V	
vThreshold	0.500 V	
rise/fall times	180 ps ±30 ps (10%, 90%)	
Probe	Agilent E5382A	

Characteristics

The characteristics are not specifications, but are included as additional information.

Table 1 Characteristics

Characteristic	Value
Maximum Conventional Timing Rate	8 GHz, quarter channel
Channel Count per Card	68
Channel Count per 5-Card Module	340
Memory Depth 16962A Option 004	4 M Samples
Memory Depth 16962A Option 016	16 M Samples
Memory Depth 16962A Option 032	32 M Samples
Memory Depth 16962A Option 064	64 M Samples
Memory Depth 16962A Option 100	100 M Samples

Environmental Characteristics

Table 2 Environmental Characteristics

Probes	
Maximum Input Voltage	± 40 V, CAT I. CAT I = Category I, secondary power line isolated circuits.
Operating Environment	
Temperature	Instrument, 0 °C to 40 °C (+32 °F to 104 °F). Note that this is the same temperature characteristic as the 16902B mainframe, but it is lower than the temperature characteristic of the 16901A mainframe, which is 0 °C to 45 °C (+32 °F to +113 °F). Probe lead sets and cables, 0 °C to 65 °C (+32 °F to 149 °F).
Humidity	Instrument, probe lead sets, and cables, up to 80% relative humidity at +40 °C (+104 °F), non-condensing.
Altitude	To 3000 m (10,000 ft).
Vibration	Operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈0.2 g (rms).
	Non-operating: Random vibration 5 to 500 Hz, 10 minutes per axis, ≈2.41 g (rms); and swept sine resonant search, 5 to 500 Hz, 0.5 g (0-peak), 5 minute resonant dwell at 4 resonances per axis. Operating power supplied by mainframe. Indoor use only. Pollution Degree 2. Normally only dry non-conductive pollution occurs. Occasionally a temporary conductivity caused by condensation may occur.

For a full listing of all specifications and characteristics, see the *Agilent 16962A Logic Analyzer Data Sheet*, literature part number 5990-3680EN, available on Agilent's web site (www.agilent.com).

Recommended Test Equipment

Table 3 Recommended Test Equipment

Equipment	Critical Specification	Recommended Model/Part	Use*
Flying Lead Probe Set (Qty 2)	No substitute	Agilent E5382A	P, T
Ground Clips (Qty 10)	No substitute	16517-82105 (pkg of 20) (Included with E5382A Probe Set)	T
Stimulus Board	No substitute	16760-60001	T
Pulse Generator	≥ 310 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent 81134A or Agilent or HP 8133A Option 003	P, T
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=250 mV.) Required for 81134A and 8133A opt. 003.	Agilent or HP 15435A	P
Oscilloscope	Bandwidth ≥ 6 GHz, sampling rate ≥ 20 GSa/s	Agilent DSO80604B or Agilent or HP 54855A	P
SMA Coax Cable (Qty 2)	>18 GHz bandwidth	Agilent or HP 8120-4948	P
Male BNC to Female SMA Adapters (Qty 2)	>18 GHz bandwidth	Cambridge Products CP-AD507 (see www.cambridgeproducts.com)	P
SMA/Flying Lead Test Connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	No substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 26	P

* P = Performance Tests, T = Troubleshooting

2 Preparing for Use

This chapter gives you instructions for preparing the logic analyzer module for use.

Power Requirements

All power supplies required for operating the logic analyzer are supplied through the backplane connector in the mainframe.

Operating Environment

The operating environment is listed on page 15. Note the non-condensing humidity limitation. Condensation within the instrument can cause poor operation or malfunction. Provide protection against internal condensation.

The logic analyzer module will operate at all specifications within the temperature and humidity range given on page 15. However, reliability is enhanced when operating the module within the following ranges:

Temperature: +20°C to +35°C (+68°F to +95°F)

Humidity: 20% to 80% non-condensing

Storage

Store or ship the logic analyzer in environments within the following limits:

- Temperature: -40°C to +75°C (-40°F to +167°F).
- Humidity: Up to 90% at 65°C (+149°F).
- Altitude: Up to 15,300 meters (50,000 feet).

Protect the module from temperature extremes which cause condensation on the instrument.

To inspect the module

1 Inspect the shipping container for damage.

If the shipping container or cushioning material is damaged, keep them until you have checked the contents of the shipment and checked the instrument mechanically and electrically.

2 Check the supplied accessories.

One or more of the accessories listed on page 12 are required to operate the 16962A logic analyzer module.

3 Inspect the product for physical damage.

Check the module and the supplied accessories for obvious physical or mechanical defects. If you find any defects, contact your nearest Agilent Technologies Sales Office. Arrangements for repair or replacement are made, at Agilent Technologies' option, without waiting for a claim settlement.

To configure and install the module

Instructions for configuring and installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900-series mainframe, go to www.agilent.com and enter "16902B" in the quick search box. In the product page's Technical Support area, select "Manuals & Guides" to find the *16900-Series Logic Analysis System Installation Guide*.

To test the module

The logic analyzer module does not require an operational accuracy calibration or adjustment. After installing the module, you can test and use the module.

- If you require a test to verify the specifications, see "Testing Logic Analyzer Performance" on page 21. If you require a test to verify correct module operation using software self-tests, see "Perform the Self-Tests" on page 24.
- If the module does not operate correctly, see "Troubleshooting" on page 63.

To clean the module

- With the mainframe turned off and unplugged, use a cloth moistened with a mixture of mild detergent and water to clean the rear panel.
- Do not attempt to clean the module circuit board.

3
Testing Logic Analyzer Performance

This chapter tells you how to test the performance of the 16962A logic analyzer against the specifications listed on page 13.

To ensure the 16962A logic analyzer (also referred to as the module or the card) is operating as specified, software tests (self-tests) and a manual performance test are done. The logic analyzer is considered performance-verified if all of the software tests and the manual performance test have passed.

The specifications for the 16962A logic analyzer define a maximum state data rate at which data can be acquired. The manual performance test (maximum state data rate test) verifies that the logic analyzer meets these specifications.

Mainframes

The 16962A logic analyzer module must be tested in a 16901A or 16902B logic analysis system frame.

The general instructions for performance test begin on page 26 with instructions for assembling the test connectors. Instructions specific to testing the module in the mainframe begin on page 40.

Test Strategy

Only specified parameters are tested. Specifications are listed on page 13. The test conditions defined in this procedure ensure that the specified parameter is as good as or better than specifications. No attempt is made to

determine performance which is better than specifications. Not all channels of the logic analyzer will be tested; a sample of channels is tested. The calibration laboratory may choose to elaborate on these tests and test all channels at their discretion.

Eye Finder is used to adjust the sampling position on every channel. Eye Finder must be used to achieve maximum state data rate performance.

The 2 Gb/s state logic analyzer will be tested. Both clocks (Clk1 and Clk3) will be tested. All four pods will be tested, one pod at a time.

The logic analyzer acquires data on both edges of the clock, so the test frequency is set to half of the acquisition speed.

One-card Module

To perform a complete test on a one-card module, start at the beginning of the chapter and follow each procedure.

Multi-card Module

To perform a complete test on a multi-card module, perform the self-tests with the cards connected. Then, remove the multi-card module from the mainframe and configure each card as a one-card module. Install the one-card modules into the mainframe and perform the performance verification tests on each card. When the tests are complete, remove the one-card modules, reconfigure them into their original multi-card module configuration, reinstall it into the mainframe and perform the self-tests again. These steps are necessary to ensure that the clocks are tested on each module.

Instructions for removing and installing the module can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900-series mainframe, go to www.agilent.com and enter "16902B" in the quick search box. In the product page's Technical Support area, select "Manuals & Guides" to find the *16900-Series Logic Analysis System Installation Guide*.

Test Interval

Test the performance of the module against its specifications at two-year intervals.

Test Record Description

A Performance Test Record for recording the results of each procedure is provided in this chapter. You may want to make a copies of this, and fill-in a copy each time you test a module.

Test Equipment

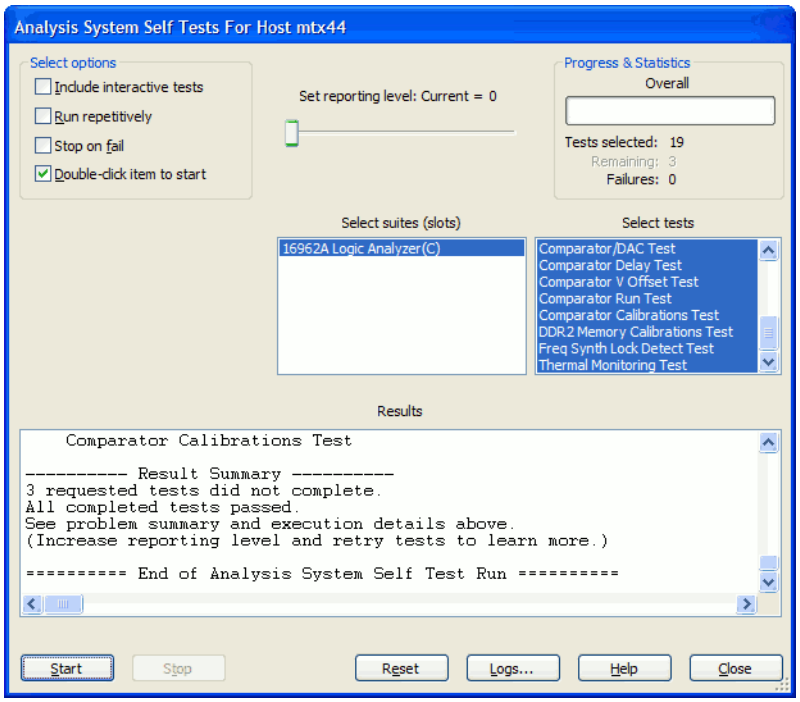
A list of the recommended test equipment is provided. You can use any equipment that satisfies the specifications given. However, the instructions are written with the presumption that you are using the recommended test equipment.

Perform the Self-Tests

When the logic analysis system has finished booting, the Waveform window appears.

1 Before performing the self-tests, disconnect all probes from the logic analyzer card.

2 Select Help→Self-Test... from the main menu. The Analysis System Self Tests window will appear.



3 In the Select suites list, select 16962A. Then, select All in the Select tests list.

4 Select Start. This will perform a complete system self-test.

5 The progress of the self tests is displayed in the Results area of the window.

6 When the self-tests are complete, check the Results window to ensure that the Result Summary says that all tests passed. If all tests did not pass, refer to "Troubleshooting" on page 63.

7 Select the Close button to close the Analysis System Self Tests window.

8 If all module self-tests pass, then record "PASS" in the "Logic Analysis System Self-Tests" section of the Performance Test Record (page 59).

Equipment Required for the Performance Test

The following equipment is required for the performance test procedure.

Table 4 Equipment Required

Equipment	Critical Specification	Recommended Model/Part
Pulse Generator	≥ 1050 MHz, two channels, differential outputs, 150-180 ps rise/fall time (if faster, use transition time converters)	Agilent 81134A or Agilent or HP 8133A option 003
150 ps Transition Time Converter (Qty 4)	Required if pulse generator's rise time is less than 150 ps. (Pulse generator conditions: Voffset=1V, ΔV=250 mV.) Required for 81134A or 8133A opt. 003.	Agilent or HP 15435A
Oscilloscope	bandwidth ≥ 6 GHz, sampling rate ≥ 20 GSa/s	Agilent DSO80604B or Agilent 54855A or similar
SMA Coax Cable (Qty 2)	>18 GHz bandwidth	Agilent or HP 8120-4948
Flying Lead Probe Set (Qty 2)	no substitute	Agilent E5382A
Male BNC to Female SMA adapters (Qty 2)		Cambridge Products CP-AD507 (see www.cambridgeproducts.com)
SMA/Flying Lead test connectors, (f) SMA to (f) SMA to Flying Lead Probe (Qty 4)	no substitute	See "Assemble the SMA/Flying Lead Test Connectors" on page 26

Assemble the SMA/Flying Lead Test Connectors

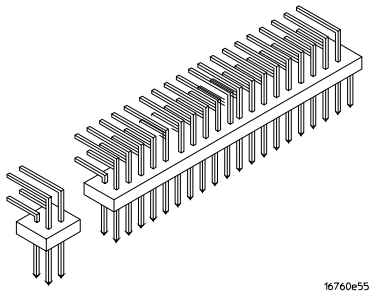
The SMA/Flying Lead test connectors provide a high-bandwidth connection between the logic analyzer and the test equipment. The following procedure explains how to fabricate the four required test connectors.

Table 5 Materials Required for SMA/Flying Lead Test Connectors

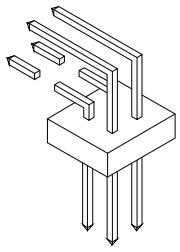
Material	Critical Specification	Recommended Model/Part
SMA Board Mount Connector (Qty 8)		Johnson 142-0701-801 (see www.johnsoncomponents.com)
Pin Strip Header (Qty 1, which will be separated)	0.100" X 0.100" Pin Strip Header, right angle, pin length 0.230", two rows, 0.120" solder tails, 2 X 40 contacts	3M 2380-5121TN or similar 2- row with 0.1" pin spacing
SMA 50 ohm terminators (Qty 2)	Minimum bandwidth 2 GHz	Johnson 142-0801-866 50 ohm Dummy Load Plug
SMA m-m adapter (Qty 4)		Johnson 142-0901-811 SMA Plug to Plug or similar

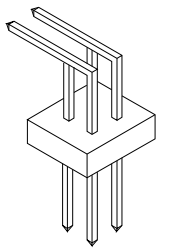
1 Prepare the pin strip header:

a Cut or cleanly break a 2 x 2 section from the pin strip.

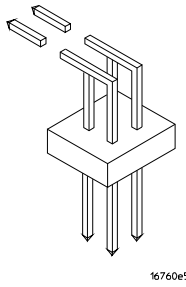


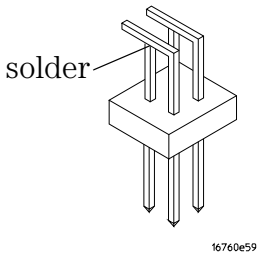
b Trim about 1.5 mm from the pin strip inner leads and straighten them so that they touch the outer leads.





c Trim about 2.5 mm from the outer leads.



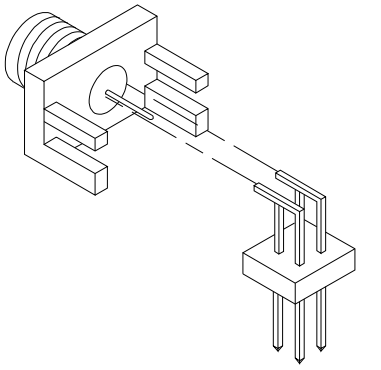


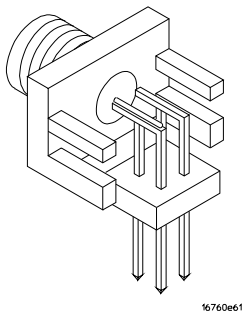
d Using a very small amount of solder, tack each inner lead to each outer lead at the point where they are touching.

2 Solder the pin strip to the SMA board mount connector:

a Solder the leads on the left side of the pin strip to the center conductor of the SMA connector as shown in the diagram below.

b Solder the leads on the right side of the pin strip to the inside of the SMA connector's frame as shown in the diagram below. Use a small amount of solder.

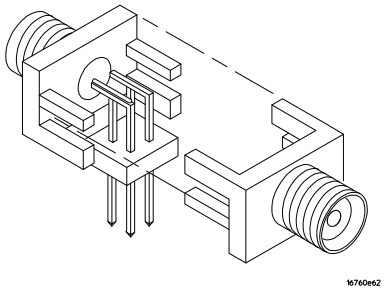


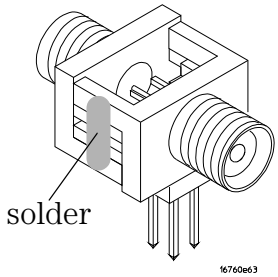


3 Attach the second SMA board mount connector:

a Re-heat the solder connection made in the previous step, and attach the second SMA connector, as shown in the diagram below. Note that the second SMA connector is upside-down, compared to the first. Add a little solder to make a good connection.

b Solder the center conductor of the second SMA connector to the center conductor of the first SMA connector and the leads on the left side of the pin strip.





c Rotate the assembly 180 degrees and solder the two SMA board mount connector frames together.

4 Check your work:

a Ensure that the following four points have continuity between them: The two pins on the left side of the pin

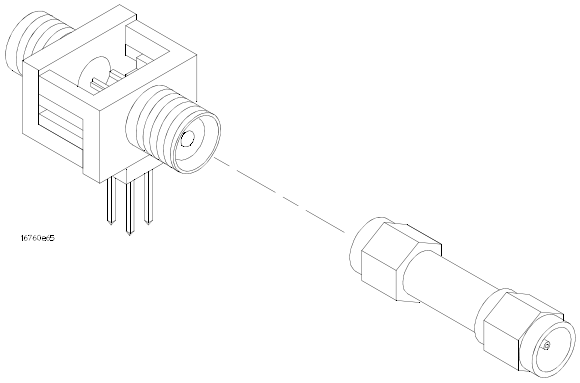
strip, and the center conductors of each SMA connector.

b Ensure that there is continuity between each of the two pins on the right side of the pin strip, and the SMA connector frames.

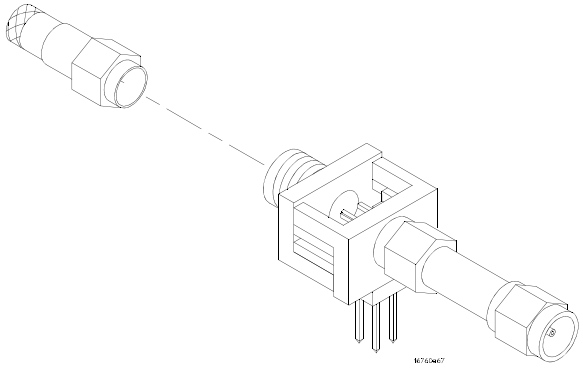
c Ensure that there is NO continuity between the SMA connector center conductor and the SMA connector frame (ground).

5 Finish creating the test connectors:

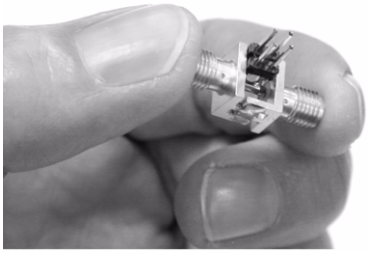
a Attach an SMA m-m adapter to one end of each of the four SMA/Flying Lead test connectors.

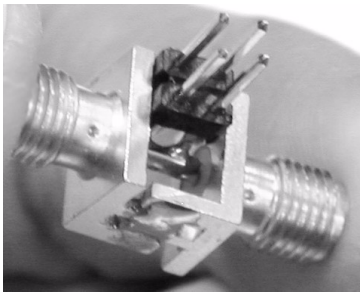


b Attach a 50 ohm terminator to the other end of two of the SMA/Flying Lead test connectors.



c The finished test connector is shown in the pictures below.





Set Up the Test Equipment

This section explains how to set up the test equipment for the minimum master-to-master clock time/maximum state data rate test.

1 Turn on the required test equipment. Let all of the test equipment and the logic analyzer warm up for 30 minutes before beginning any test.

2 Set up the pulse generator according to one of the following tables.

   a Set the frequency of the pulse generator:

   In this test procedure, the logic analyzer uses both edges of the clock to acquire data. The test frequency is half the test clock rate because data is acquired on both the rising edge and the falling edge of the clock. Set the frequency to 1000 MHz plus 2% (1020 MHz). This includes the frequency uncertainty of the pulse generator, plus a test margin.

   For example, if you are using an 8133A pulse generator, the frequency accuracy is ±0.5% of setting.

   If you are using an 81134A pulse generator, the frequency accuracy is ±0.005% of setting.

   b Set the rest of the pulse generator parameters to the values shown in one of the following tables.

Table 6 81134A Pulse Generator Setup

Main	Channel 2	Channel 1	Trigger
Mode: Pulse/Pattern	Mode: Square ÷ 1	Mode: Square ÷ 1	Disable
Freq: set in previous step.	**Timing**	**Timing**	
Clock Internal	Delay Ctrl Input Off	Delay Ctrl Input Off	
	Width: (not available in square mode)	Width: (not available in square mode)	
	Pulse Perf: Normal	Pulse Perf: Normal	
	Deskew: 0 ps	Deskew: 0 ps	
	Levels: Normal, Custom	**Levels: Normal, Custom**	
	Ampl: 0.25 V	Ampl: 0.25 V	
	Offset: 0.5 V	Offset: 0.5 V	
	Term Voltage: 0 mV	Term Voltage: 0 mV	
	Limit to current Levels: unselected	Limit to current Levels: unselected	
	Output: Enable (LED on)	Output: Enable (LED on)	
	$\overline{\text{Output}}$: Enable (LED on)	$\overline{\text{Output}}$: Enable (LED on)	

Table 7 8133A Pulse Generator Setup

Timebase	Pulse Channel 2	Trigger	Pulse Channel 1
Mode: Int	Mode: Square ÷ 1	Disable (LED on)	Mode: Square
Freq: was set in previous step.	Delay: (not available in pulse mode)		Delay: 0 ps
	Width: (not available in square mode)		Width: (not available in square mode)
	Ampl: 0.25 V		Ampl: 0.25 V
	Offs: 0.5 V		Offs: 0.5 V
	Output: Enable (LED off)		Output: Enable (LED off)
	Comp: Normal (LED off)		Comp: Normal (LED off)
	Limit: Off (LED off)		Limit: Off (LED off)
	$\overline{\text{Output}}$: Enable (LED off)		$\overline{\text{Output}}$: Enable (LED off)

3 Set up the oscilloscope.

a Set up the oscilloscope according to one of the following tables.

Table 8 DSO80604B Oscilloscope Setup

Setup: Channel 1	Setup: Channel 2	Setup: Channel 3	Setup: Channel 4
On	On	Off	Off
Scale: 50 mV/div	Scale: 50 mV/div		
Offset: 500 mV	Offset: 500 mV		
Skew: (Set later. See page 38.)	Skew: 0.0 seconds		

Setup: Horizontal	Setup: Trigger	Setup: Acquisition	Setup: Display
Scale: 200 ps	Mode: Edge	Sampling Mode: Real Time	**Waveforms**
Position: 0 s	Source: Channel 1	Memory Depth: Automatic	Connect dots
Reference: Center	Level: 500 mV	Averaging: Enabled	Color Grade: not selected
External 10 MHz Reference Clock: not selected	Edge: Rising Edge	# of Averages: 16	Infinite Persistence: not selected
Roll Mode: not selected	Sweep: Auto	Bandwidth: 6 GHz	Waveform Brightness: as preferred
Delayed: not selected			**Grid**: On, Quantity: 1
			Intensity: as preferred

Measure: Markers
Mode: Manual placement
All else: (n/a)

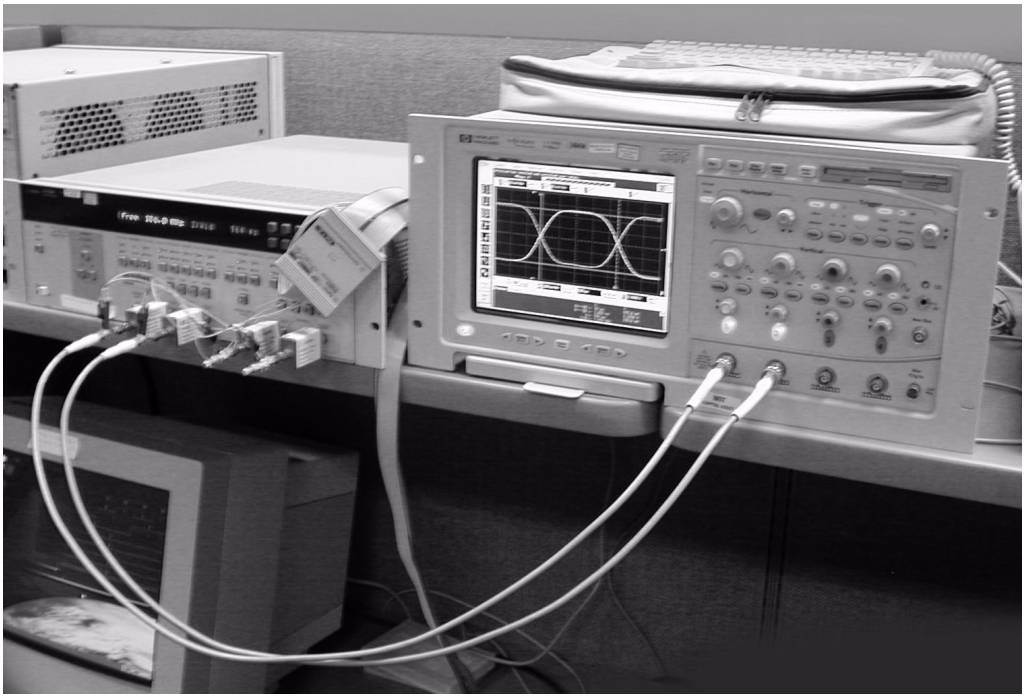
Table 9 54855A Oscilloscope Setup

Setup: Channel 1	Setup: Channel 2	Setup: Channel 3	Setup: Channel 4
On	On	Off	Off
Scale: 50 mV/div	Scale: 50 mV/div		
Offset: 500 mV	Offset: 500 mV		
Skew: (Set later. See page 38.)	Skew: 0.0 seconds		

Setup: Horizontal	Setup: Trigger	Setup: Acquisition	Setup: Display
Scale: 200 ps	Mode: Edge	Sampling Mode: Real Time	**Waveforms**
Position: 0 s	Source: Channel 1	Memory Depth: Automatic	Connect dots: checked
Reference: Center	Level: 500 mV	Sampling Rate: Automatic	Display Mode: Normal
Roll Mode: not selected	Edge: Rising Edge	Sine(x)/x Interpolation: checked	Persistence: Minimum
Delayed: not selected	Sweep: Auto	Averaging: Enabled, # of Averages: 16	Waveform Brightness: as preferred
		Bandwidth: Automatic	**Grid**: On, Quantity: 1, Intensity: as preferred

Measure: Markers
Mode: Manual placement
All else: (n/a)

Connect the Test Equipment

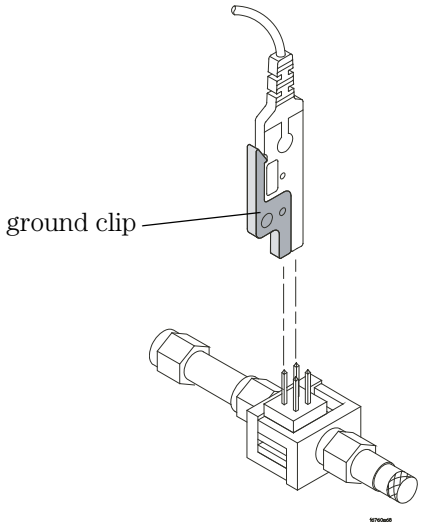


Connect the 16962A Logic Analyzer Pod to the Pulse Generator

1. Connect Transition Time Converters (if required–see page 25) to each of the four outputs of the pulse generator: Channel 1 OUTPUT, Channel 1 $\overline{\text{OUTPUT}}$, Channel 2 OUTPUT, Channel 2 $\overline{\text{OUTPUT}}$.
2. Connect the two SMA/Flying Lead test connectors (see "Assemble the SMA/Flying Lead Test Connectors" on page 26) *with* 50 ohm terminators to the Transition Time Converters at the pulse generator Channel 1 OUTPUT and Channel 1 $\overline{\text{OUTPUT}}$. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
3. Connect the two SMA/Flying Lead test connectors *without* 50 ohm terminators to the Transition Time Converters at the pulse generator Channel 2 OUTPUT and Channel 2 $\overline{\text{OUTPUT}}$. (If Transition Time Converters are not required, connect the SMA/Flying Lead test connectors directly to the pulse generator outputs.)
4. Connect one E5382A Flying Lead Probe Set to Pod 1 of the 16962A logic analyzer. This probe set is used for data inputs.

5 Connect the other E5382A Flying Lead Probe Set to Pod 3 of the 16962A logic analyzer. This probe set is used for the clock input.

6 Connect the Pod 3 E5382A Flying Lead Probe Set's CLK lead to the pin strip of the SMA/Flying Lead connector at the pulse generator's Channel 1 OUTPUT.

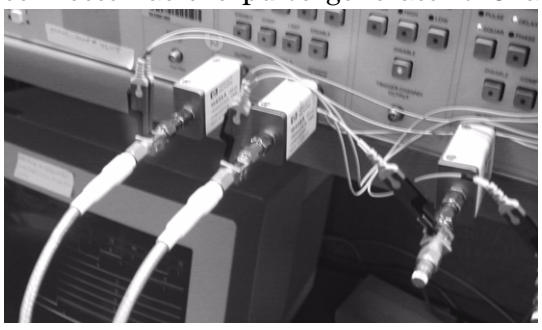


NOTE Be sure to use the black ground clip (supplied with the E5382A Flying Lead Probe Set) and orient the leads so that the black clip is connected to one of the SMA/Flying Lead connector's ground pins!

7 Connect the Pod 3 E5382A Flying Lead Probe Set's $\overline{\text{CLK}}$ lead to the SMA/Flying Lead connector at the pulse generator's Channel 1 $\overline{\text{OUTPUT}}$. Again, be sure to use the black ground clip and orient the leads so that the black clip is connected to ground.

8 Connect the Pod 1 E5382A Flying Lead Probe Set's bits 2 and 10 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 $\overline{\text{OUTPUT}}$.

9 Connect the Pod 1 E5382A Flying Lead Probe Set's bits 6 and 14 to the SMA/Flying Lead test connector's pin strip connector at the pulse generator's Channel 2 OUTPUT.

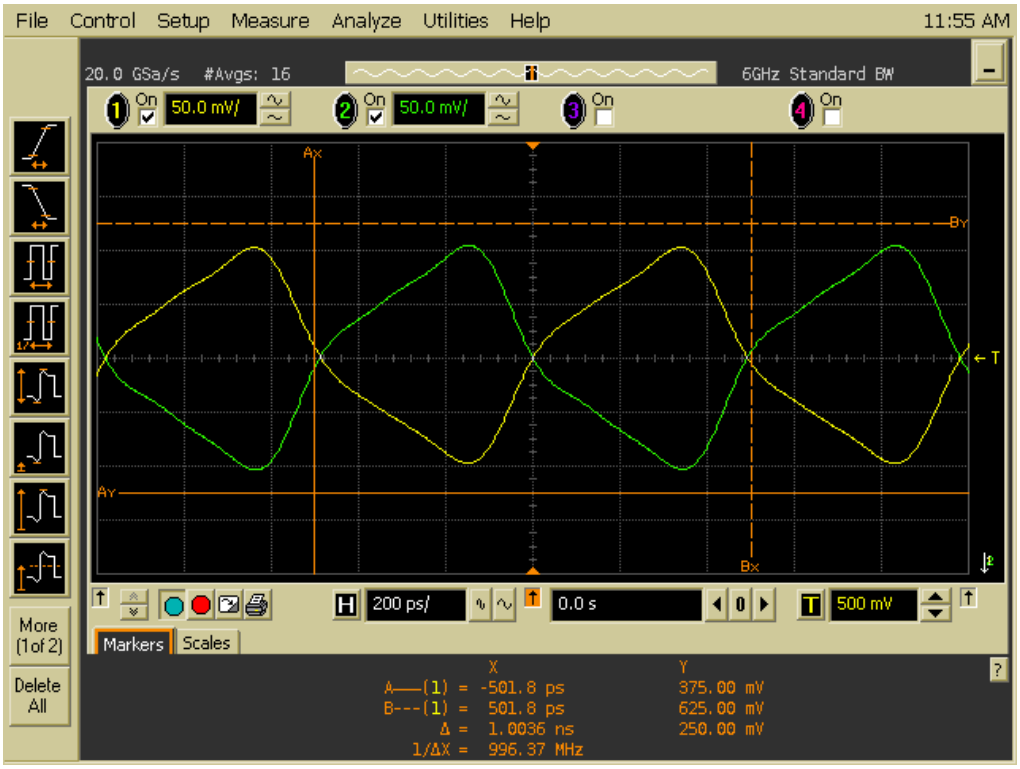


Connect the Pulse Generator Output to the Oscilloscope

1. Attach Male BNC to Female SMA adapters to Channels 1 and 2 on the oscilloscope.
2. Attach one end of an SMA cable to the Male BNC to Female SMA adapter on Channel 1 of the oscilloscope.
3. Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 OUTPUT of the pulse generator.
4. Attach one end of the other SMA cable to the Male BNC to Female SMA adapter on Channel 2 of the oscilloscope.
5. Attach the other end of the SMA cable to the SMA/Flying Lead connector at the Channel 2 $\overline{\text{OUTPUT}}$ of the pulse generator.

Verify and adjust the pulse generator DC offset

1. On the oscilloscope, select Measure from the menu bar at the top of the display.
2. Select Markers...
3. In the Markers Setup window set marker “Ay” to 375 mV, and set marker “By” to 625 mV.



4 Observe the waveforms on the oscilloscope display. If they are not centered within the “Ay” and “By” markers, adjust the pulse generator’s Channel 2 OFFSET until the waveforms are centered as well as possible.

(The resolution of the 8133A pulse generator is 20 mV, and the resolution of the 81134A pulse generator is 10 mV.)

Deskew the oscilloscope

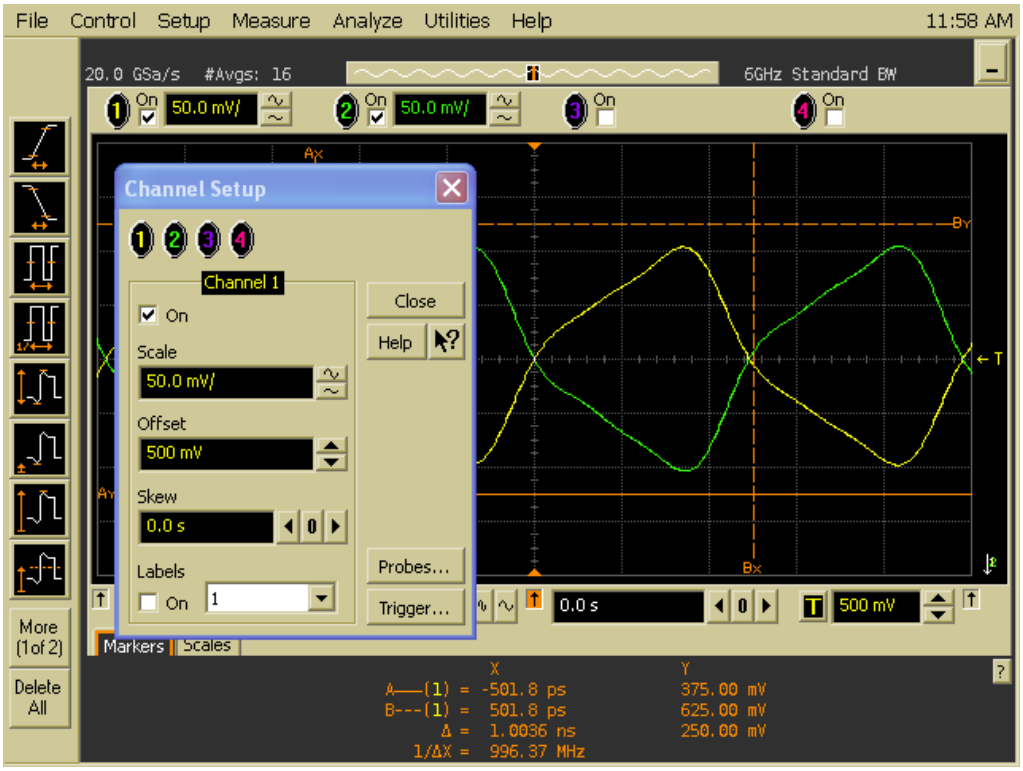
This procedure neutralizes any skew in the oscilloscope’s waveform display.

1 On the oscilloscope, make sure the Horizontal scale is 200 ps/div. You can do this using the large knob in the Horizontal setup section of the front panel.

2 Select Setup from the menu bar at the top of the display.

3 Select Channel 1.

4 Click Skew </> to deskew Channel 1 and Channel 2 signals so that both channels cross the horizontal center line at the same time, at both ends of the eye (both crossings of the horizontal center line). The horizontal center of the graticule line is at 500 mV because the vertical offset was set to 500 mV in the oscilloscope setup described on page 33.



5 Select Close in the Channel Setup window.

Testing the Module

The following sections explain how to test the maximum state data rate.

1 Record the 16962A logic analyzer's model and serial number in the Performance Test Record (see page 59). Record your work order number (if applicable) and today's date.

2 Record the test equipment information in the "Test Equipment Used" section of the Performance Test Record.

3 Turn on the logic analysis system.

NOTE Before testing the performance of the module, warm-up the logic analyzer and the test equipment for 30 minutes.

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a Optionally, connect a keyboard and mouse to the rear panel of the mainframe.

b Plug in the power cord to the power connector on the rear panel of the mainframe.

c Turn on the main power switch on the mainframe front panel.

While the logic analysis system is booting, observe the boot dialogue for the following:

- Ensure all of the installed memory is recognized.
- Any error messages.
- Interrupt of the boot process with or without error message.

4 During initialization, check for any failures.

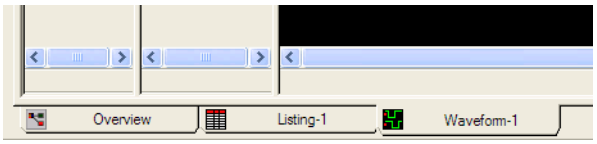
If an error or an interrupt occurs, refer to the Agilent Technologies *16900-Series Logic Analysis System Service Guide* for troubleshooting information.

Configure the Logic Analysis System

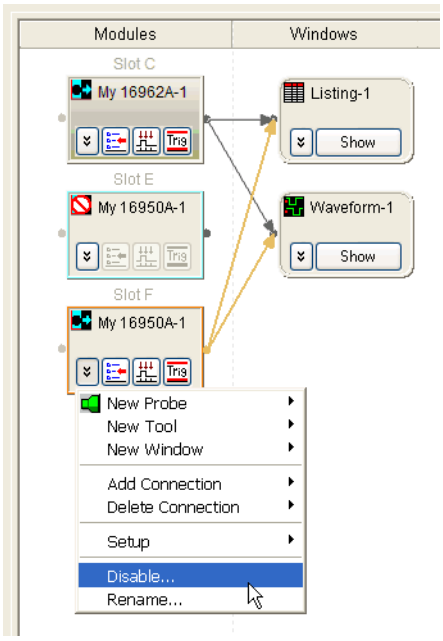
1 In the *Agilent Logic Analyzer* application, choose File→New. This puts the logic analysis system into its initial state.

2 Disable all logic analyzers other than the analyzer under test.

a Select the Overview tab at the bottom of the main window.

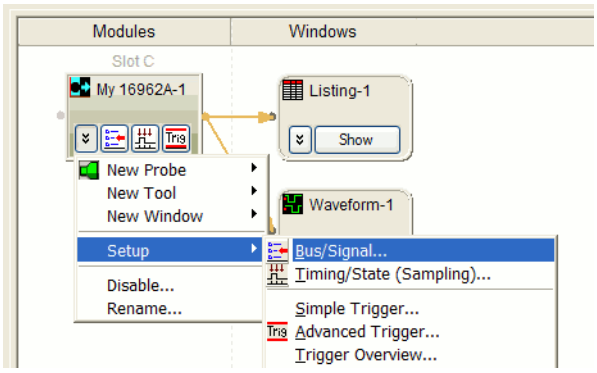


b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.



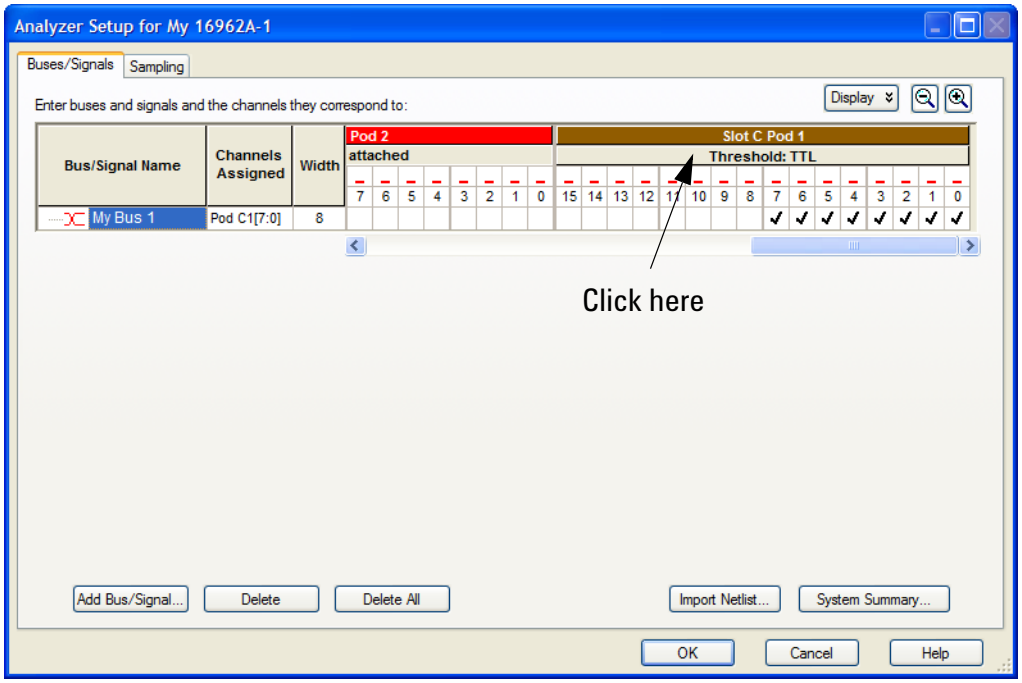
3 Set up the bus and signals:

a In the Overview window, select Setup→Bus/Signal... from the module's drop-down menu.

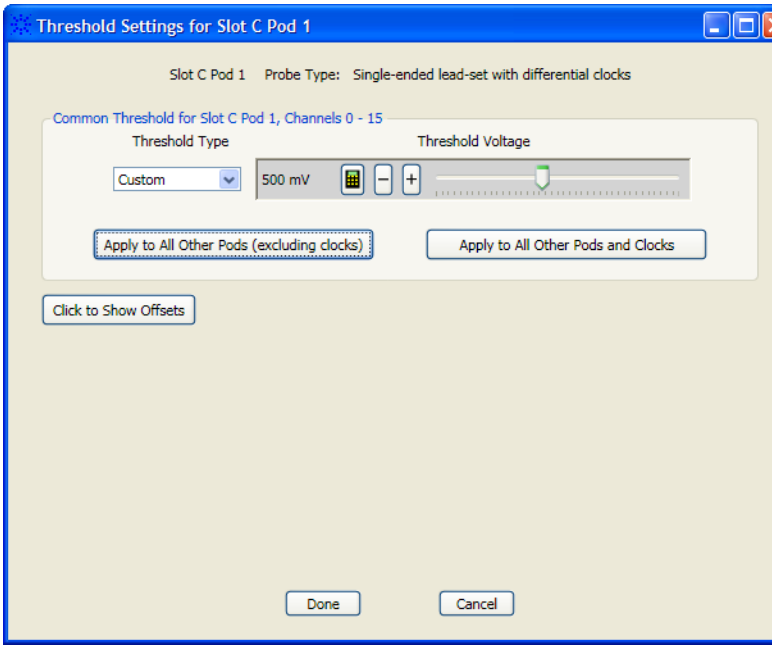


b In the Analyzer Setup window, choose the Threshold button for Pod 1. The Threshold Settings window will appear.

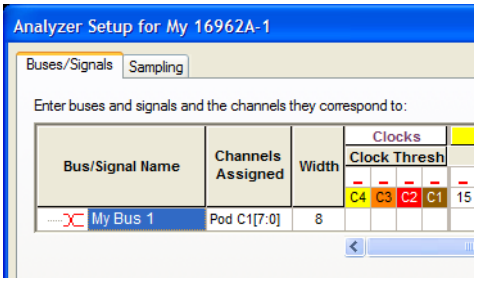
NOTE The E5382A probe must be connected to the logic analyzer pod as described on page 35.



c Set the threshold value for Pod 1 of the logic analyzer to 500 mV. Click Apply to All Other Pods (Excluding Clocks). Then, click Done to close the dialog.



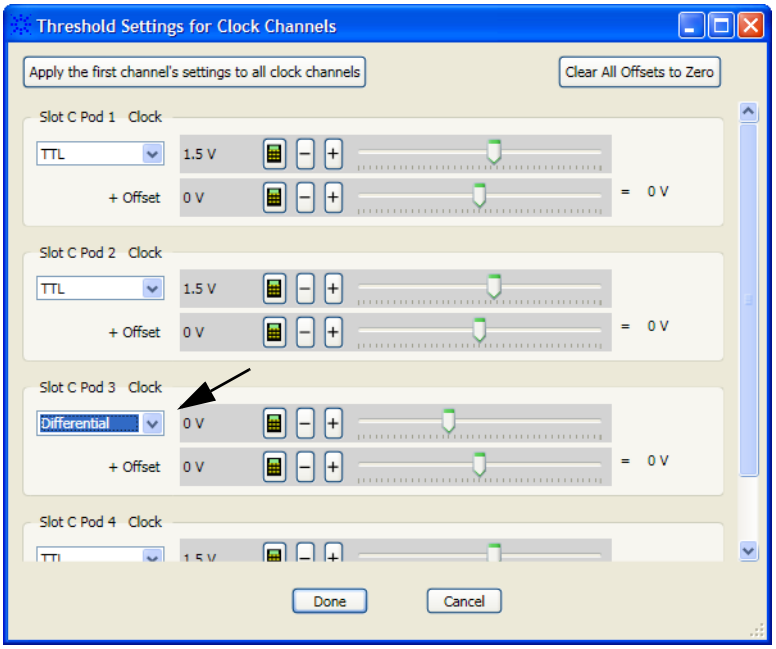
d Drag the scroll bar all the way to the left.



e Select the Clock Thresholds button.

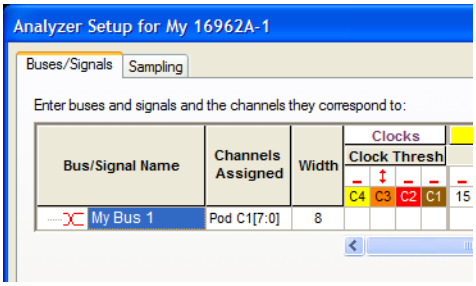
f In the Threshold Settings for Clock Channels dialog, set

the Pod 3 clock threshold to Differential.



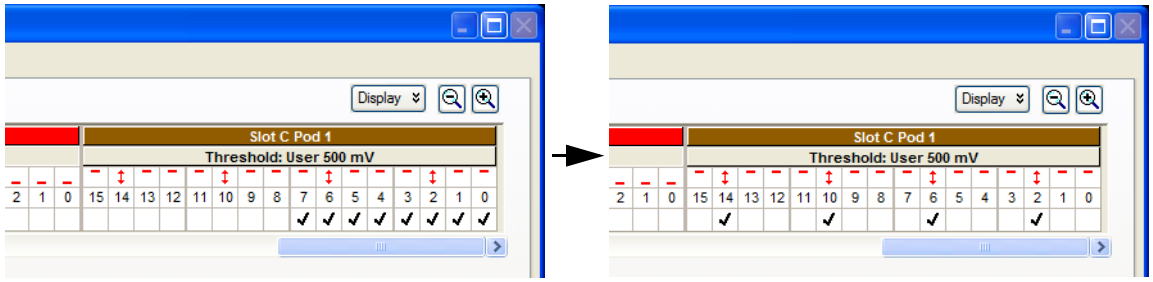
Click Done.

The activity indicator will show activity on clock 3.



g The activity indicators now show activity on the channels that are connected to the pulse generator. Un-assign all channels. Hint: you can do this quickly by clicking on the left-most check mark and dragging to the right across all of the other check marks. If you

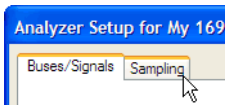
have a logic analysis system with a touchscreen, you can drag across with your finger.



h Click (or touch) to select channels 2, 6, 10, and 14 as shown in the picture above.

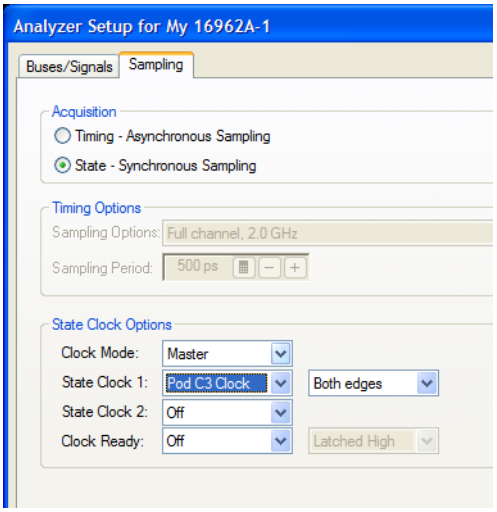
4 Select the State sampling mode and set the State Clock options:

a Select the Sampling tab of the Analyzer Setup window.



b Select State - Synchronous Sampling.

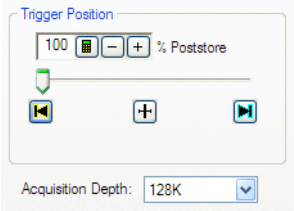
c For State Clock 1, select Pod 3 Clock and Both edges.



5 Set the trigger position and acquisition memory depth:

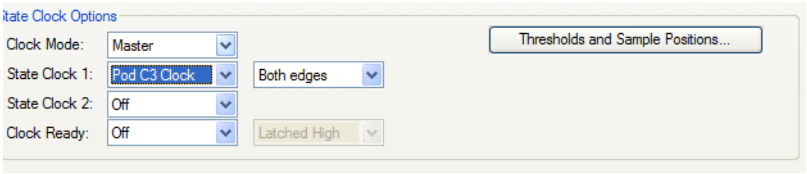
a Set the Trigger Position to 100% Poststore.

b Set the Acquisition Depth to 128K.



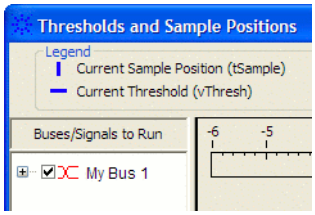
Adjust sampling positions using Eye Finder

1 Select the Thresholds and Sample Positions button.

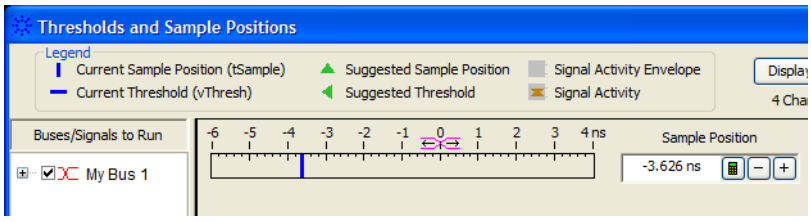


The Thresholds and Sample Positions dialog will appear.

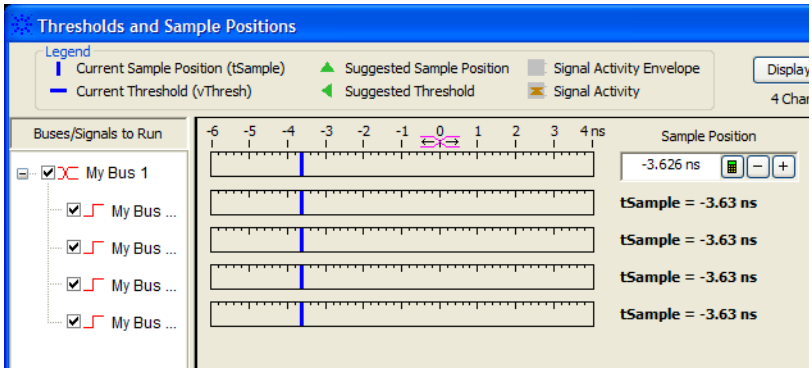
2 In the “Buses/Signals” section of the Thresholds and Sample Positions dialog, ensure that the check box next to “My Bus 1” is checked.



3 Drag the blue bar for “My Bus 1” to approximately -3.6 ns.



4 Select the plus sign to expand bus “My Bus 1”.



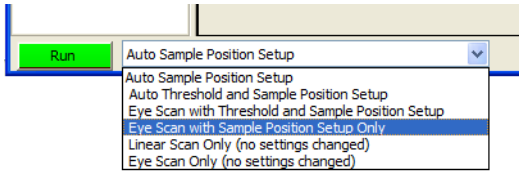
NOTE

Align the blue bars vertically

Initially, the blue bars will be vertically aligned. After running Eye Finder, the blue bars will not be vertically aligned because an independent sample position will be determined for each channel.

1 If the blue bars in the Eye Finder display are not vertically aligned:
   a In the “My Bus 1” row, grab the right-most blue bar with the mouse pointer and move it all the way to the left. Release the mouse button. This will vertically align all of the blue bars.
2 Using the mouse pointer, grab the blue bar for “My Bus 1 (4 channels)” and move it to the recommended starting position of -3.6 ns. All of the blue bars will follow.

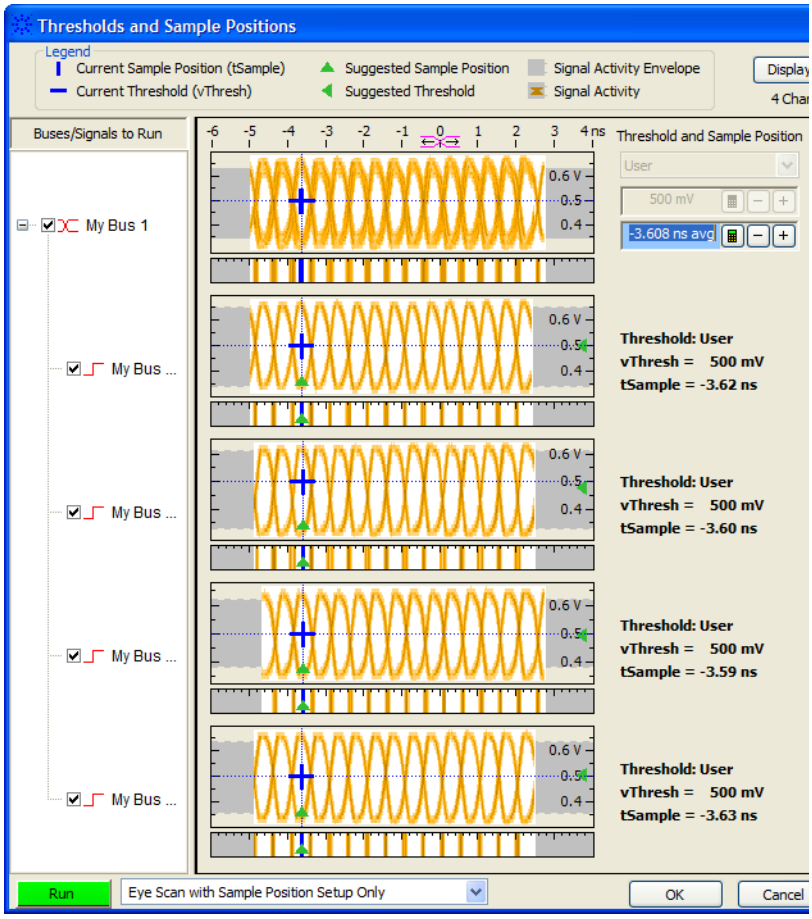
5 Select the Eye Scan with Sample Position Setup Only run type.



6 Select the Run button in the Thresholds and Sample Positions dialog.

7 Ensure that an eye appears for each bit near the recommended starting position. Depending on your test setup, the eye position may vary. Any skew between channel 1 and channel 2 of your pulse generator will cause the eye position to shift to the left or right in the Eye Finder display. A shift of up to 0.5 ns should be considered normal. The important point is that your Eye Finder display should look similar to the picture below

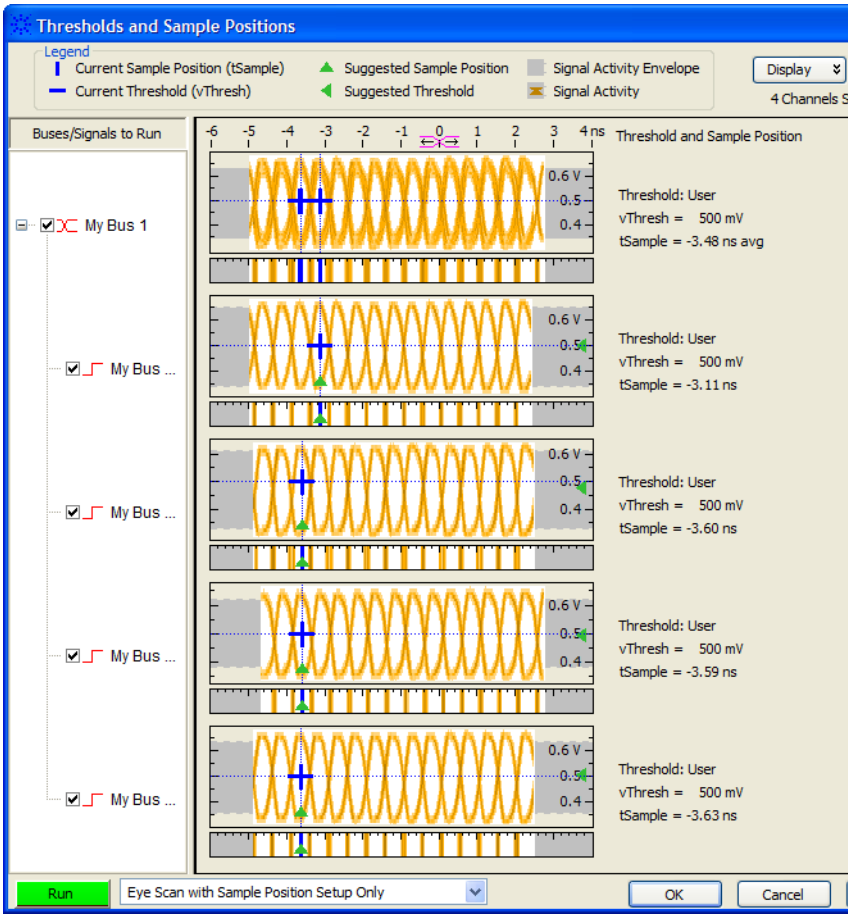
(although it may be shifted left or right), and Eye Finder must be able to place the blue bars in the eye.



To re-align a stray channel

If the blue bar for a particular bit does not appear in its eye near the recommended starting position, then do the following steps to realign the sampling position of the stray

channel. In the following example, the sampling position of one channel (My Bus 1 [0]) must be realigned with the sampling position of the other channels.

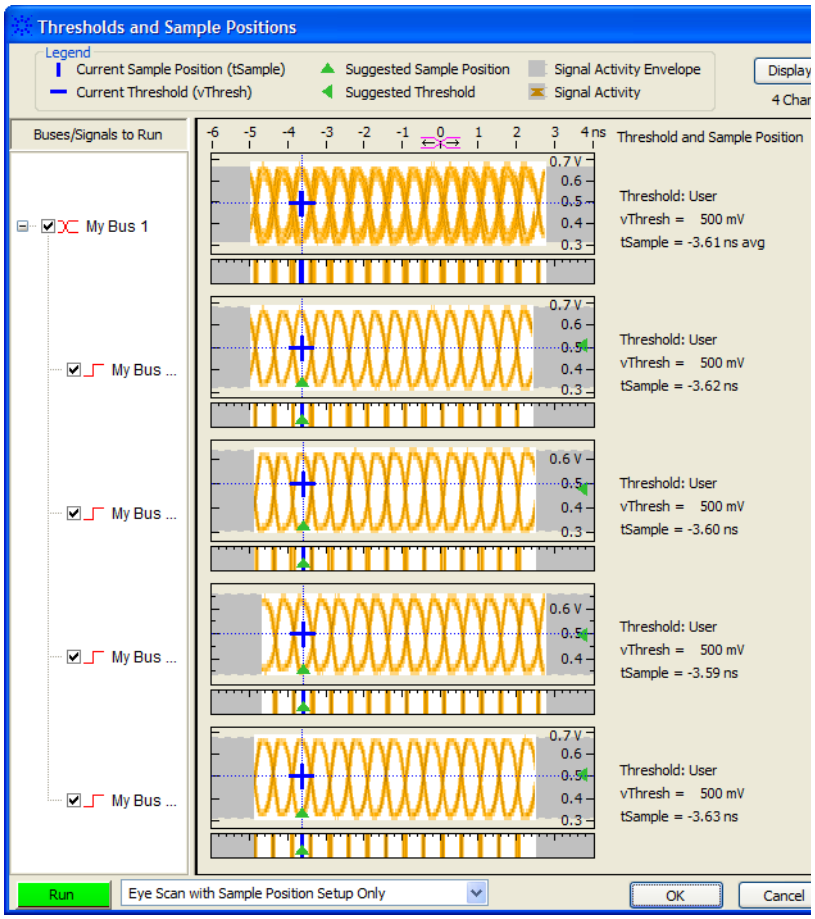


1 Using the mouse, drag the sample position (blue line) of a stray channel (channel “My Bus 1 [0]” in the above example) so that it is in the same eye as the other channels. The Suggested Position from Eye Finder (green triangle) will also move to the new eye.

2 Repeat the above step for all remaining stray channels.

3 Select the Run button in the Thresholds and Sample Positions dialog. Eye Finder will recalculate the new sample positions based on the sample position changes.

The following example shows all sampling positions aligned and in the correct eye.



Test Pod 1

The steps that follow include pass/fail criteria.

Determine PASS/FAIL (1 of 2 tests)

1 PASS/FAIL: If an eye exists near -3.6 ns for every bit, and Eye Finder places a blue bar in the narrow eye for each bit, then the logic analyzer passes this portion of the test. Record the result in the "Eye Finder locates an eye for each bit" section of the Performance Test Record (page 59).

2 If an eye does not exist near -3.6 ns for every bit or Eye Finder cannot place the blue bar in the narrow eye, then the logic analyzer fails the test. Record the result in the "Eye Finder locates an eye for each bit" section of the Performance Test Record (page 59).

Close the Eye Finder and Analyzer Setup Windows

1 Select OK to close the Thresholds and Sample Positions dialog.

2 Select OK to close the Analyzer Setup window.

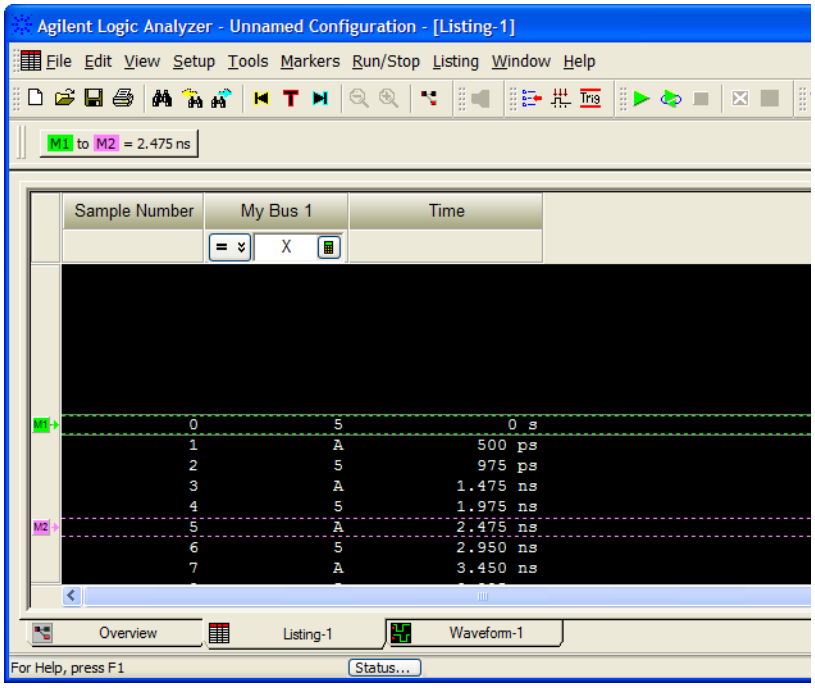
Configure the markers

Data must be acquired before the markers can be configured. Therefore, you need to run the analyzer to acquire data.

1 Switch to the Listing window by selecting the Listing tab at the bottom of the main window.

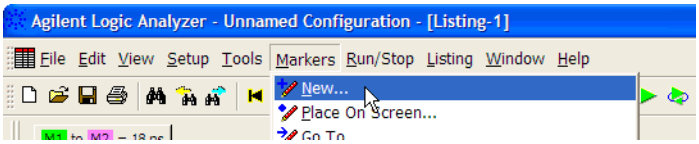
2 Select the Run icon  .

3 Data will appear in the Listing Window upon completion of the run.

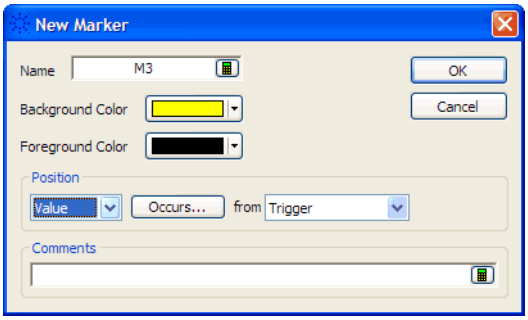


If the data values are not “A”s and “5”s, you may need to set the sampling positions in different eyes.

4 From the Main Menu choose Markers→New.



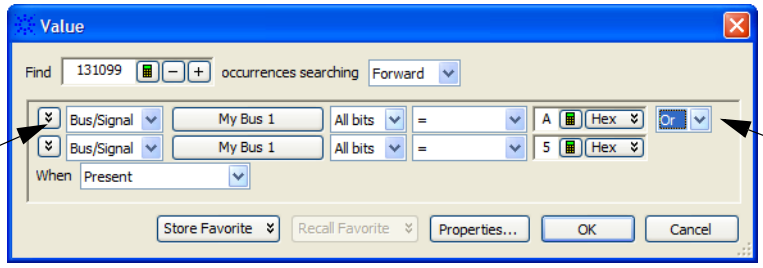
a You can accept the default name for the new marker.



b Change the Position field to Value.

c Select the Occurs... button and create the marker setup shown below.

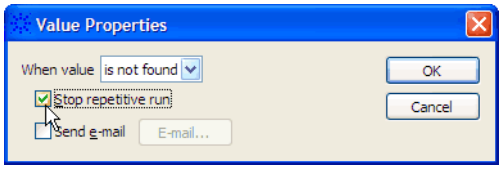
Click here to add event



Click here to select "Or"

5 In the Value window, select the Properties... button.

6 In the Value Properties window, select Stop repetitive run when value is not found.



7 Select OK to close the marker Value Properties window.

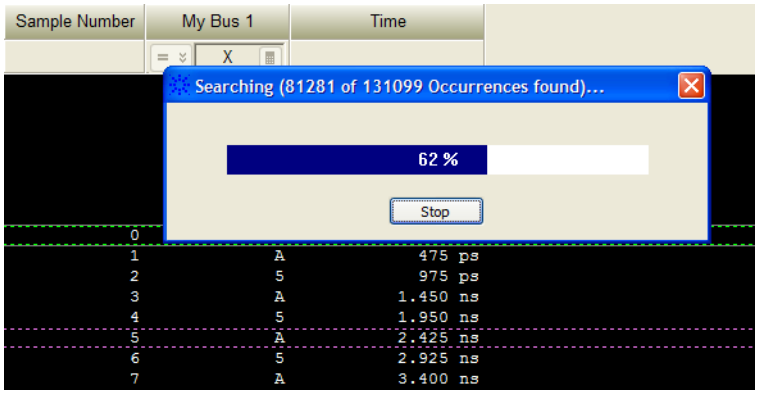
8 Select OK to close the marker Value window. The system will search the display for the occurrences specified.

9 Select OK to close the New Marker window.

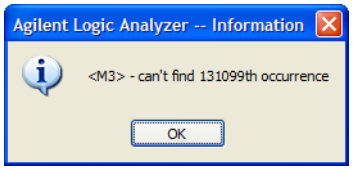
Determine PASS/FAIL (2 of 2 tests)

Pass/Fail Point: The Listing window is set up to search for the appropriate number of A's and 5's in the acquisition. If the logic analyzer does not detect the correct number of A's and 5's, an error window will appear.

1 Select the Run Repetitive icon . Let the logic analyzer run for about one minute. The analyzer will acquire data and the Listing Window will continuously update.



If the "can't find occurrence" window appears, then the logic analyzer fails the test.



Check your test setup. If the failure is not the result of a problem with the test setup, record the failure in the "Maximum State Data Rate" section of the Performance Test Record.

NOTE Be sure that the black ground clip is making good contact with the ground pin on the test connector.

2 After about one minute, select the Stop button to stop the acquisition.

If the "can't find occurrence" window does not appear, then the analyzer passes the test. Record "Pass" in the "Maximum State Data Rate" section of the Performance Test Record.

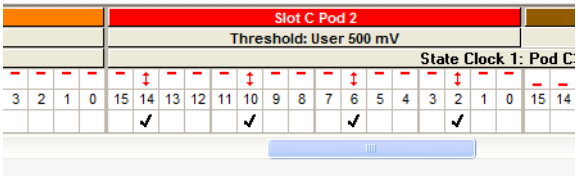
Test the complement of the bits

Now test the logic analyzer using inverted levels (in other words, complement data).

1 On the pulse generator, in the PULSE setup for CHANNEL 2, select inverted levels:
   - On the 81134A pulse generator, select Levels: Inverted.
   - On the 8133A pulse generator, select COMP (LED on).
2 Verify the DC offset and adjust it if necessary. See page 37.
3 Adjust the sampling positions (run Eye Finder). See page 46.
4 Determine pass or fail (1 of 2 tests). See page 50.
5 Switch to the Listing window by selecting the Listing tab at the bottom of the main logic analyzer window.
6 Select the Run Repetitive icon  .
7 Determine pass or fail (2 of 2 tests). See page 53.

Test Pod 2

1 Disconnect the E5382A Flying Lead Probe Set from Pod 1 and connect it to Pod 2 of the logic analyzer. (The clock input on Pod 3 remains the clock input when testing Pod 2.)
2 On the pulse generator, in the PULSE setup for CHANNEL 2, return the outputs to normal (non-inverted or non-complement) levels.
3 Verify the DC offset and adjust it if necessary. See page 37.
4 In the Overview window, select Setup→Bus/Signal... from the module's drop-down menu.
5 Scroll to the right and unassign all Pod 1 bits.
6 Set the Pod 2 threshold to 500 mV (just as you did for Pod 1 on page 43).
7 Assign bits 2, 6, 10, and 14 of Pod 2.



8 Adjust the sampling positions using Eye Finder. Be sure to expand “My Bus 1” and use the recommended starting position noted on page 46. Realign any stray channels if necessary. See page 48.

9 Determine pass or fail (1 of 2 tests). See page 50.

10 Select OK to close the “Analyzer Setup” window.

11 Switch to the Listing window by selecting the Listing tab at the bottom of the main logic analyzer window.

12 Select the Run Repetitive icon  .

13 Determine pass or fail (2 of 2 tests). See page 53.

Test the complement of the bits (Pod 2)

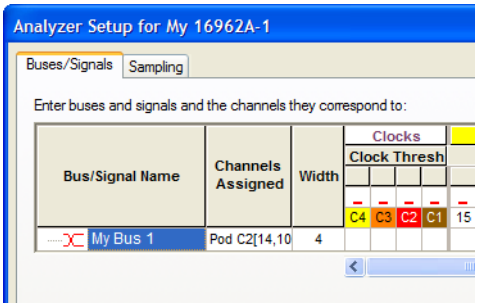
1 Test the complement of the bits. See page 54.

Test Pods 3 and 4

1 Disconnect the E5382A Flying Lead Probe Set from Pod 3 and connect it to Pod 1 of the logic analyzer. (The clock input on Pod 1 is used when testing Pod 3 and Pod 4.)

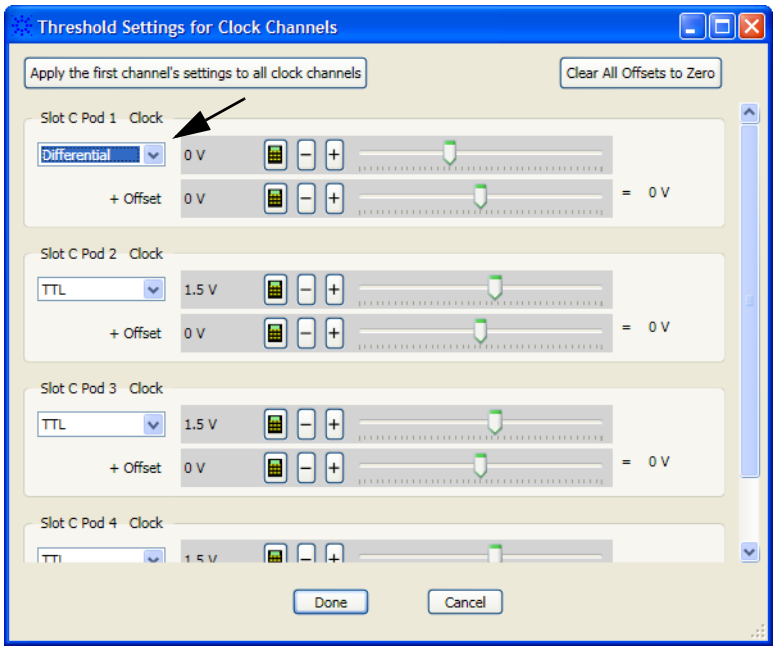
2 In the Buses/Signals setup dialog, set the Pod 1 clock threshold to Differential:

a Drag the scroll bar all the way to the left.



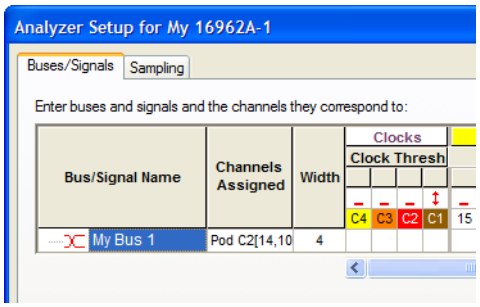
b Select the Clock Thresholds button.

c In the Threshold Settings for Clock Channels dialog, set the Pod 1 clock threshold to Differential.



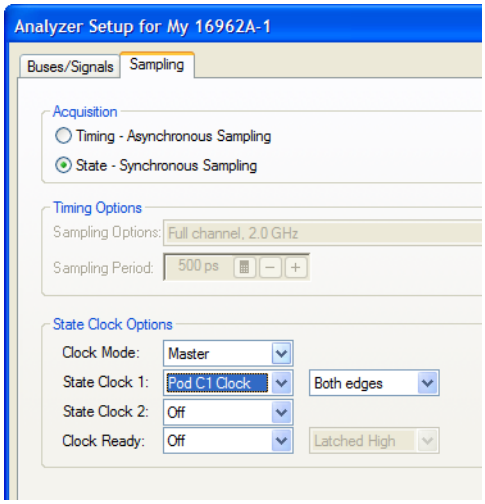
Click Done.

The activity indicator will show activity on clock 1.



3 Set the State Clock options:

a For State Clock 1, select Pod 1 Clock and Both edges.



4 Perform the normal and complement tests for Pod 3 and Pod 4, changing the connection to the pod, setting thresholds, making channel assignments, etc., as appropriate.

Upon completion, the logic analyzer is completely tested.

Conclude the State Mode Tests

Do the following steps to properly shut down the logic analyzer session after completing the state mode tests.

1 End the test.

a From the Main Menu, choose File→Exit. At the dialog "Do you want to save the current configuration?" select No.

Ending and restarting the logic analysis session will re-initialize the system.

b Disconnect all cables and adapters from the pulse generator and the oscilloscope.

Performance Test Record

LOGIC ANALYZER MODEL NO. (circle one): 16962A

Logic Analyzer Serial No.	Work Order No.
Date:	Recommended Test Interval - 2 Year/4000 hours
	Recommended next testing:

TEST EQUIPMENT USED

Pulse Generator Model No.	Oscilloscope Model No.
Pulse Generator Serial No.	Oscilloscope Serial No.
Pulse Generator Calibration Due Date:	Oscilloscope Calibration Due Date:

MEASUREMENT UNCERTAINTY

Clock Rate	
Pulse Generator Frequency Accuracy: 81134A: ±0.005% of setting. 8133A: ±0.5% of setting. 2% = uncertainty + at least 1% test margin.	
Setting 1000 MHz + 2% = 1020 MHz	

TEST RESULTS

Logic Analysis System Self-Tests (Pass/Fail):		
Performance Test: Maximum State Data Rate		
Pulse Generator Settings	Freq: 1000 MHz plus 2% (1020 MHz).	
	Square wave.	
Test Criteria	Test 1 of 2 Eye Finder locates an eye for each bit	Test 2 of 2 Correct number of occurrences detected
Pod 1 Results (pass/fail):		
Pod 2 Results (pass/fail):		
Pod 3 Results (pass/fail):		
Pod 4 Results (pass/fail):		

4 Calibrating

This chapter gives you instructions for calibrating the logic analyzer.

Calibration Strategy

The 16962A logic analyzer does not require any periodic adjustments or calibration by the user to ensure operational accuracy.

However, Agilent recommends that performance of the 16962A logic analyzer be tested against its specifications at two-year intervals (see “Testing Logic Analyzer Performance" on page 21). This testing is required in order to obtain calibration certification.

5 Troubleshooting

This chapter helps you troubleshoot the module to find defective assemblies.

The troubleshooting consists of flowcharts, self-test instructions, and a cable test.

If you suspect a problem, start at the top of the first flowchart. During the troubleshooting instructions, the flowcharts will direct you to perform the self-tests or the cable test.

The service strategy for this instrument is the replacement of defective assemblies. This module can be returned to Agilent Technologies for all service work, including troubleshooting. Contact your nearest Agilent Technologies Sales Office for more details.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wrist-straps and mats when you perform any service to this instrument or to the modules in it.

To use the flowcharts

Flowcharts are the primary tool used to isolate defective assemblies. The flowcharts refer to other tests to help isolate the trouble. The circled numbers on the charts indicate connections with the other flowchart. Start your troubleshooting at the top of the first flowchart.

Mainframe Operating System

Before troubleshooting a 16962A module, ensure that the required version of mainframe operating system is installed on the mainframe. The required operating system software versions are listed in “Mainframe and Operating System" on page 12.

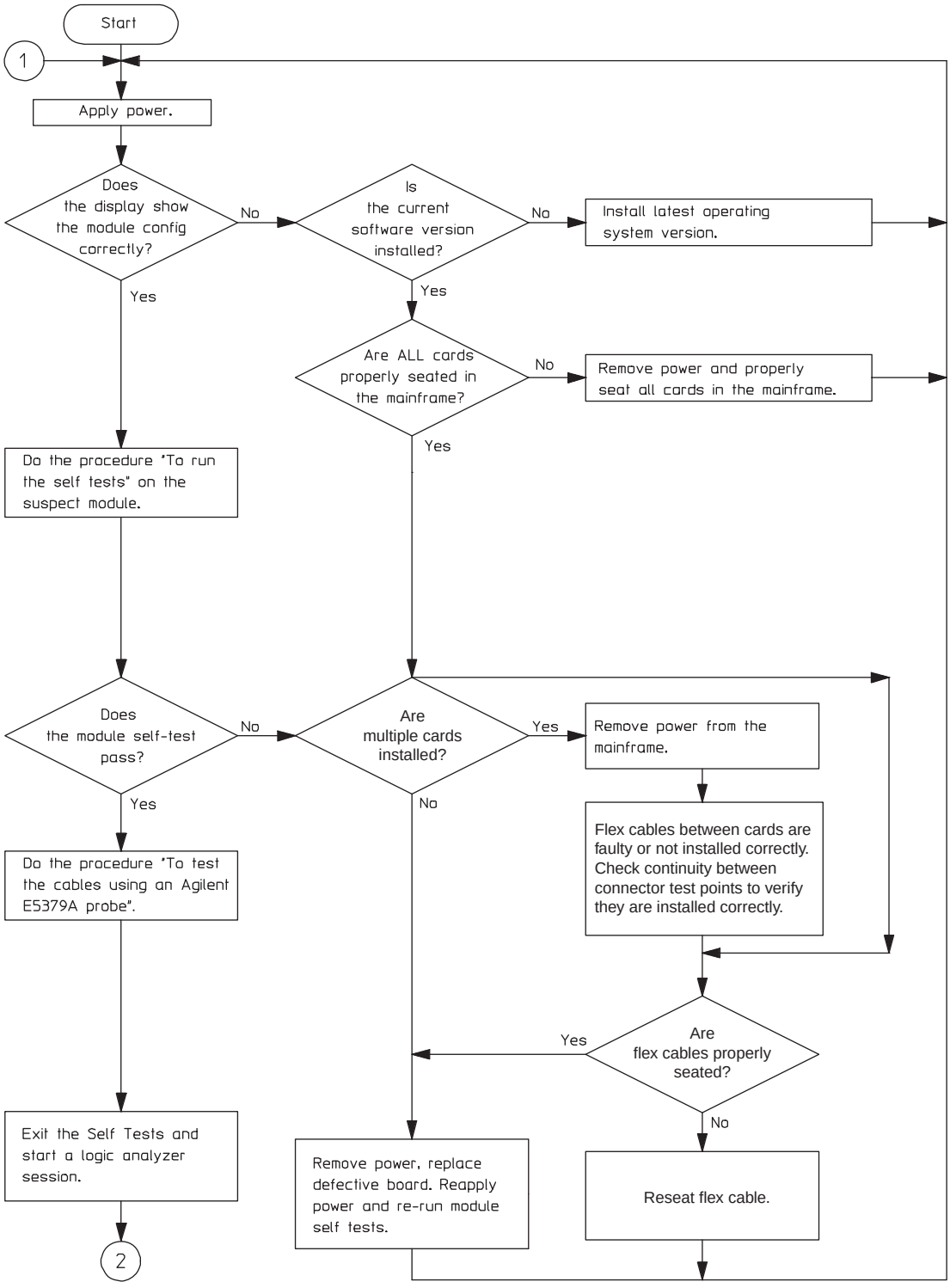


Figure 1 Troubleshooting Flowchart 1

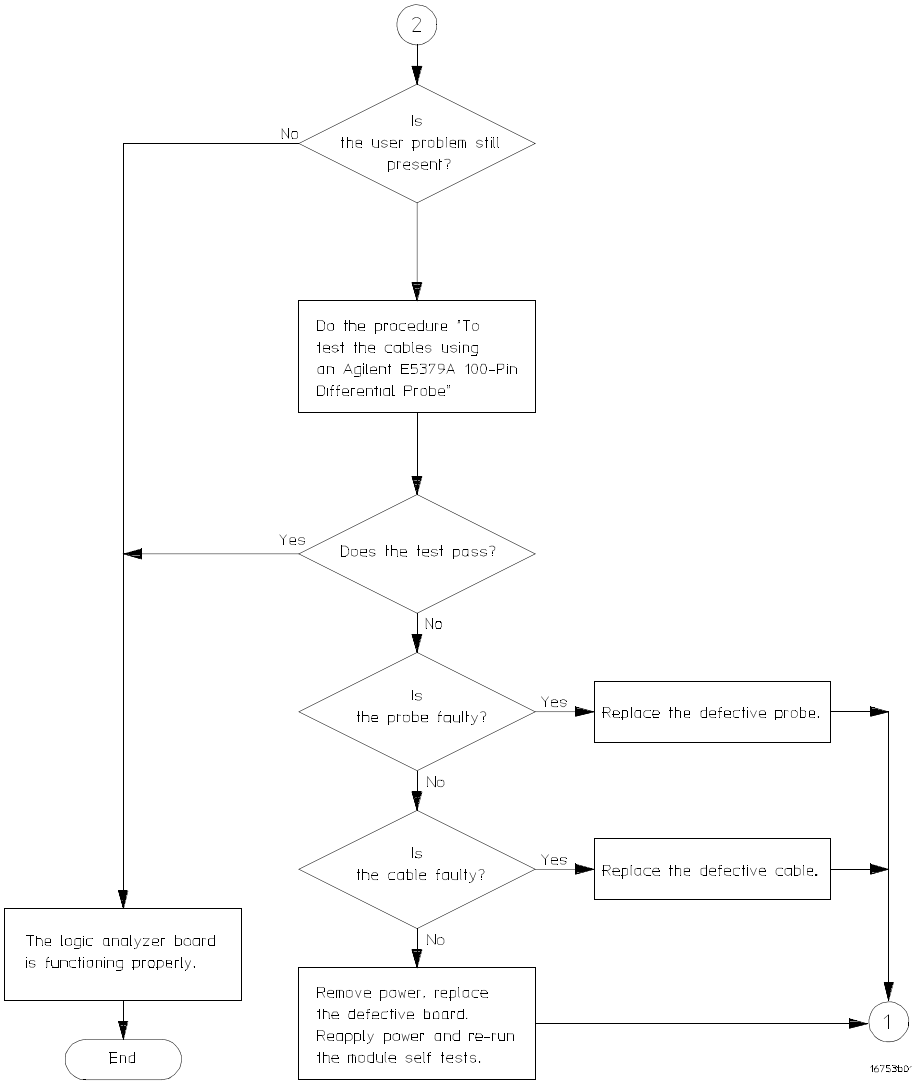


Figure 2 Troubleshooting Flowchart 2

To run the self tests

1 See “Perform the Self-Tests" on page 24.

Self-Test Descriptions

The self-tests for the logic analyzer identify the correct operation of major functional areas in the module.

PC Board Revision Test

This tests that the FPGA is communicating with the backplane and that the board under test is a supported version.

Interface FPGA Version Test

This test verifies that the FPGA program is a version that the software can use. This is necessary because new features will be added to the 16962A that will require both new software and new FPGA bits.

Interface FPGA Register Test

The purpose of this test is to verify that the backplane interface can communicate with the backplane FPGA. The FPGA must be working before any of the other circuits on the board will work. Also, the FPGA generates the board ID code that is returned to identify the module and slot.

FPGA to FPGA Communication Test

This test is only run if there are two or more 16962A logic analyzer cards connected together with the flex cables. The purpose of this test is to verify that the FPGAs can drive and receive the signals correctly.

Resource Bus Connection Test

This test is only run if there are two or more 16962A logic analyzer cards in adjacent slots in the frame.

This test makes sure that the flex cables are squarely and firmly inserted into the connectors.

EEPROM Test

The purpose of this test is to verify:

- The address and data paths to the EEPROM.
- That each cell in the EEPROM can be programmed high and low.
- That individual locations can be independently addressed.
- The EEPROM can be block erased.

ADC Test

The purpose of this test is to verify that the three test voltages can be properly read from the Analog to Digital converter. This verifies that the ADC reference voltages are properly connected and that the correct data can be read from the device.

Probe ID Read Test

The purpose of this test is to verify that the Probe ID values can be correctly read and to verify the functionality of the Digital to Analog Converter by testing the two Probe ID DAC outputs at various voltage levels.

DMA Test

The purpose of this test is to verify the high-speed transfer of data from the Analysis chip to the FPGA.

Chip Registers Read/Write Test

The purpose of this test is to verify that each bit in each register of the Analysis chip can be written with a 1 and 0 and read back again. The test also verifies that a chip reset sets all registers to their reset condition (all 0s for most registers).

Comparator Programming Test

The purpose of this test is to verify the programming path to each of the comparators.

Comparator/DAC Test

This test is executed only if all probes are detached.

This test uses the pod, bonus, and calibration DACs, the calibration oscillator (implemented in the interface FPGA), the comparators, the connections between the comparators and the Analysis chip, and the activity indicators in the Analysis chip. We verify that we can use the DACs to control the data input to the comparators. We verify that each comparator data channel produces output. We verify that each comparator output is connected to each ASIC data input.

Comparator Delay Test

The comparator delay test verifies the integrity of all the delay line elements for each delay line in the comparators. Each delay line consists of 11 delay elements. When set for maximum delay, all 11 elements are connected in series. If any element is faulty, then data will not propagate through the comparator. If this is the only test failing, then it is almost certainly a bad comparator.

Comparators V Offset Test

This test will not be executed if any probes are attached to any of the probe cables. This test verifies that the V Offset (offset null) taps for each data channel of each comparator can be independently programmed and that each tap has the expected effect on the V Offset adjustment. The tap settings are programmable inside each comparator chip. If this is the only test failing, then it is almost certain that is a bad comparator.

Comparator Run Test

The purpose of the Comparator Run Test is to verify some specific paths through the comparator used during the start of a run are working correctly.

Comparator Calibrations Test

The purpose of this test is to verify that each of the comparator one-time calibrations can successfully be performed. This verifies that all of the calibration circuitry and components are within the tolerance limits required for proper calibration. This test is executed only if all probes are detached.

DDR2 Memory Calibrations Test

This test runs the Acquisition IC's DDR2 calibrations and determines if any fail.

Freq Synth Lock Detect Test

This test determines if all the voltage-controlled oscillators (VCOs) are working properly.

Thermal Monitoring Test

The purpose of the Thermal Monitoring Test is to verify that none of the monitored components are above their "limit" temperature.

To exit the test system

1 Simply close the self-test window. No additional actions are required.

To test the cables

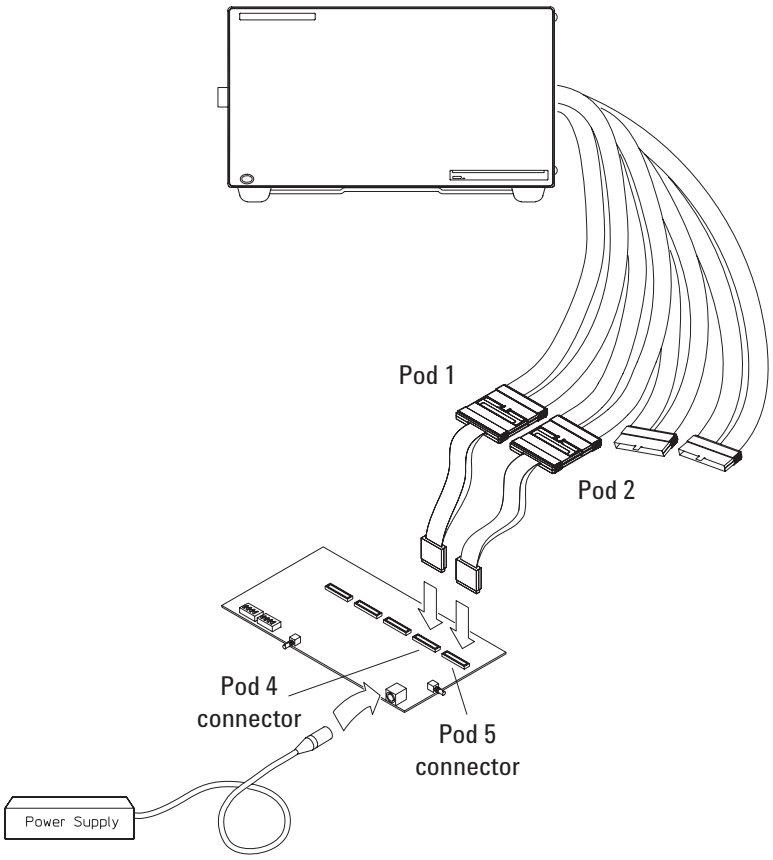
This test allows you to functionally verify logic analyzer cables and Agilent E5379A probes.

Table 10 Equipment Required to Test Cables

Equipment	Critical Specification	Recommended Part
Stimulus Board	No Substitute	16760-60001
Differential Probes	No Substitute	E5379A (Qty 2)

1 Connect the logic analyzer to the stimulus board.

- **a** Connect the Agilent E5379A 100-pin differential probes to the logic analyzer cable (also called “Pods”) to be tested. Start with Pods 1 and 2.
- **b** Connect the E5379A probe from logic analyzer Pod 1 to connector “Pod 4” on the stimulus board.
- **c** Connect the E5379A probe from logic analyzer Pod 2 to connector “Pod 5” on the stimulus board.
- **d** Connect the stimulus board power supply output to the stimulus board power supply connector J82.
- **e** Plug in the stimulus power supply to line power. The green LED DS1 should illuminate showing that the stimulus board is active.



2 Set up the stimulus board

   a Configure the oscillator select switch S1 according to the following settings:

      • S1 0 (Off).
      • S2 1 (On).
      • S3 0 (Off).
      • Int.

   b Configure the data mode switch S4 according to the following settings:

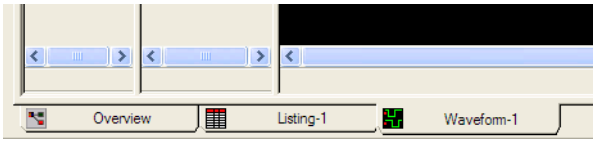
      • Even.
      • Count.

   c Press the Resynch VCO button, then the Counter RST (Counter Reset) button.

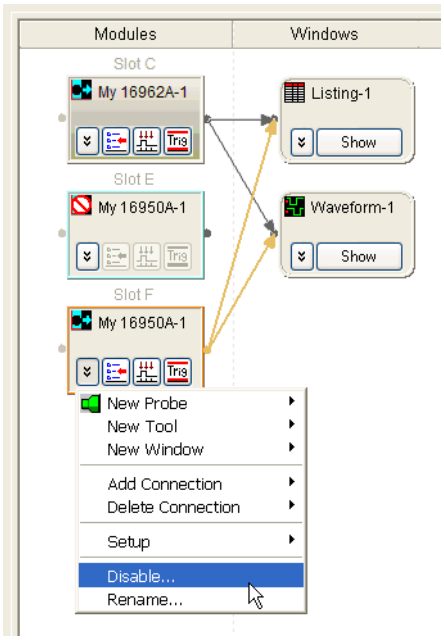
3 In the *Agilent Logic Analyzer* application, choose File→New. This puts the logic analysis system into its initial state.

4 Disable all analyzers except the one being tested. This simplifies the instructions and makes module initialization faster.

a Select the Overview tab at the bottom of the main window.

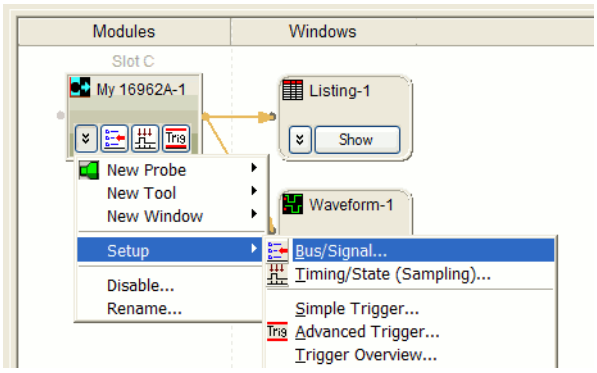


b Click on each unused logic analyzer and select disable. Only the logic analyzer to be tested should remain enabled.

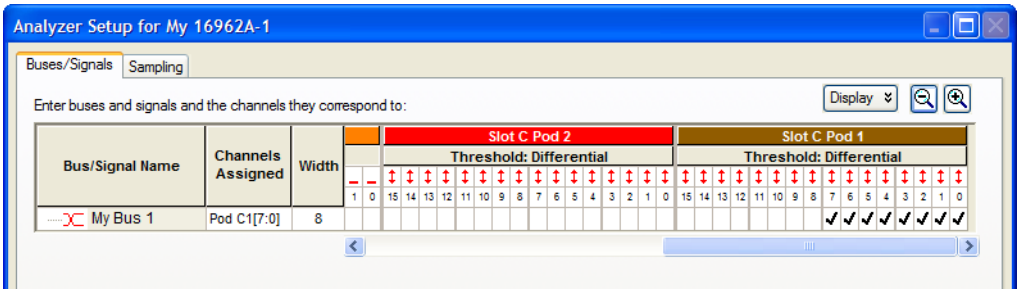


5 Set up the bus:

a In the Overview window, select Setup→Bus/Signal... from the module's drop-down menu.

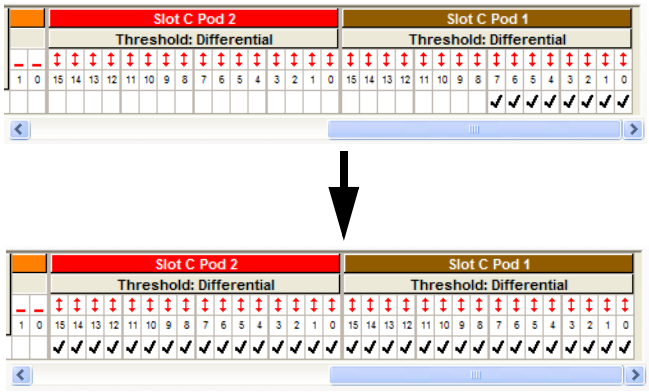


b Scroll if necessary to view the pods you are testing.



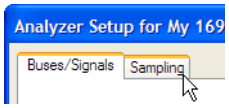
c Verify that the pod threshold buttons say "Threshold: Differential", as shown above. If they don't, make sure the correct probes (E5379A) are attached to pods 1 and 2. The threshold is set to Differential automatically when E5379A probes are attached.

d Channels 7 through 0 are already assigned by default. Assign pod 2 channels 15 through 0 and pod 1 channels 15 through 8 by clicking and dragging from the left-most channel box to the right-most channel box. Your display should look like the lower picture when you are done.



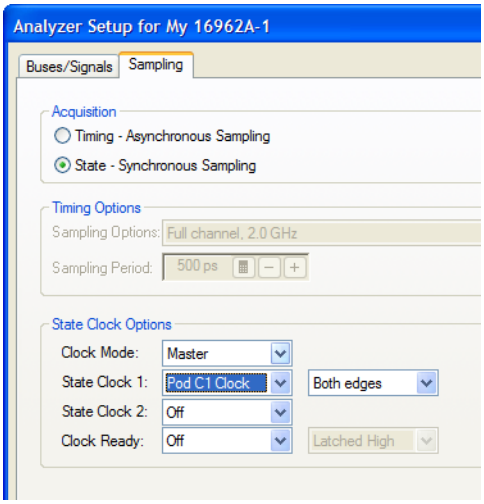
6 Select the State sampling mode and set the State Clock options:

a Select the Sampling tab of the Analyzer Setup window.



b Select State - Synchronous Sampling.

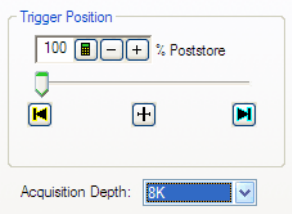
c For State Clock 1, select Pod 1 Clock and Both edges.



7 Set the trigger position and acquisition memory depth:

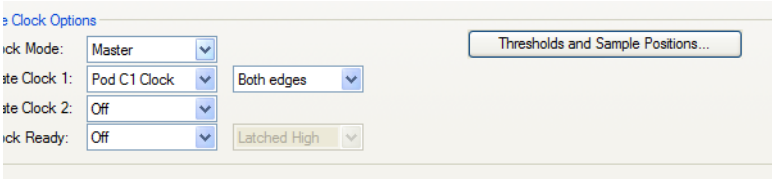
a Set the Trigger Position to 100% Poststore.

b Set the Acquisition Depth to 8K.

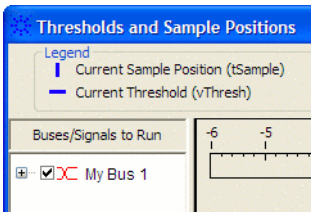


8 Adjust sampling positions:

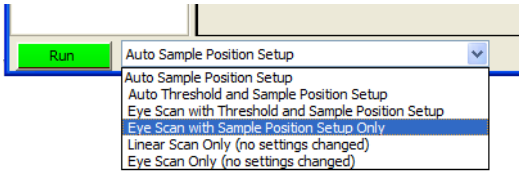
a Select the Thresholds and Sample Positions button. The Thresholds and Sample Positions dialog will appear.



b In the “Buses/Signals” section of the Thresholds and Sample Positions dialog, make sure the check box next to “My Bus 1” is checked.

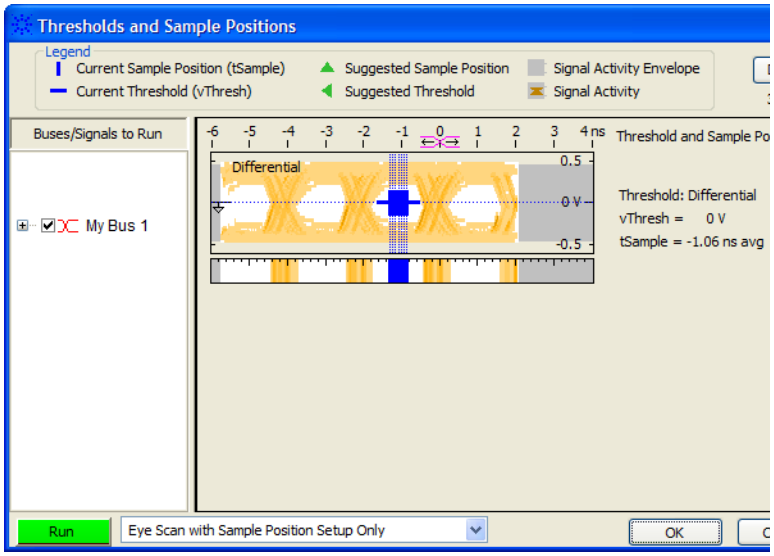


c Select the Eye Scan with Sample Position Setup Only run type.



d Select the Run button in the Thresholds and Sample Positions dialog.

e Make sure the sampling positions are set properly, and re-align any stray channels if necessary (see page 48).

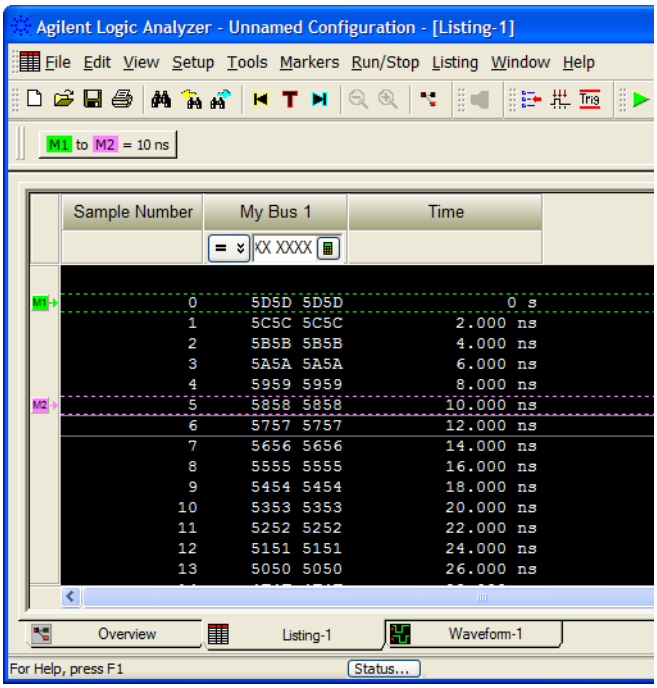


f Select OK to close the Thresholds and Sample Positions window.

g Select OK to close the Analyzer Setup window.

9 Switch to the Listing window by selecting the Listing tab at the bottom of the main window.

10 Select the Run icon  . The listing should look similar to the figure below when you scroll down a bit.



Scroll down at least 256 samples to verify the data. My Bus 1 shows four 8-bit binary counters decrementing by 1. If the listing does not look similar to the figure, there is a possible problem with the cable or probe. Cause for cable test failures include:

- Open channel.
- Channel shorted to a neighboring channel.
- Channel shorted to either ground or a supply voltage.

If the test data is not correct, then perform the following step to isolate the failure.

11 Verify the failure:

a Swap the E5379A probes so that the pod 1 cable remains connected to the stimulus board's pod 4 connector and the pod 2 cable remains connected to the stimulus board's pod 5 connector — just using different probes.

b Select the Run icon  .

If the failure is the same (that is, the error follows the cable) then the cable is suspect.

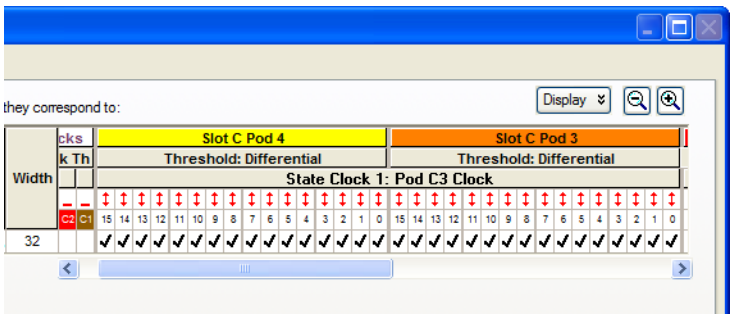
If the failure switches pods (that is, the error follows the E5379A probe) the probe is suspect.

12 Repeat the cable test for pods 3 and 4:

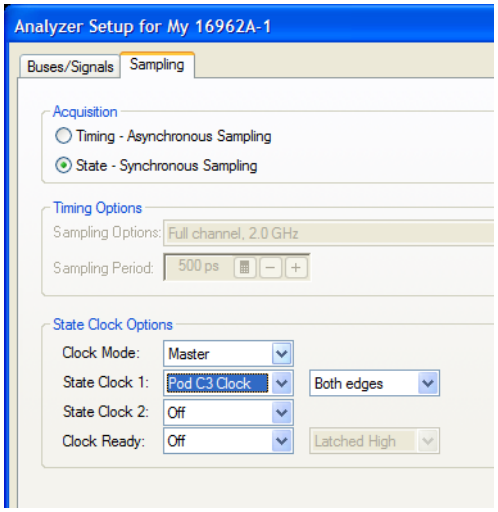
a Connect the logic analyzer's pod 3 cable to the stimulus board's pod 4 connector.

b Connect the logic analyzer's pod 4 cable to the stimulus board's pod 5 connector.

c In the Buses/Signals tab of the Analyzer Setup window, assign the pod 3 and 4 channels to "My Bus 1".



d In the Sampling tab of the Analyzer Setup window, for State Clock 1, select Pod 3 Clock and Both edges.



e Adjust sampling positions.

f Select the Run icon  . In the Listing window, check at least 256 samples for failures; if necessary, verify any failures by swapping the E5379A probes.

Return to the troubleshooting flowchart.

6 Replacing Assemblies

This chapter contains the instructions for removing and replacing the logic analyzer module, the circuit board of the module, and the probe cables of the module as well as the instructions for returning assemblies.

CAUTION Turn off the instrument before installing, removing, or replacing a module in the instrument.

CAUTION Electrostatic discharge can damage electronic components. Use grounded wriststraps and mats when performing any service to this module.

Tools Required

- A T10 TORX screwdriver is required to remove screws connecting the probe cables and screws connecting the back panel.

To remove the module

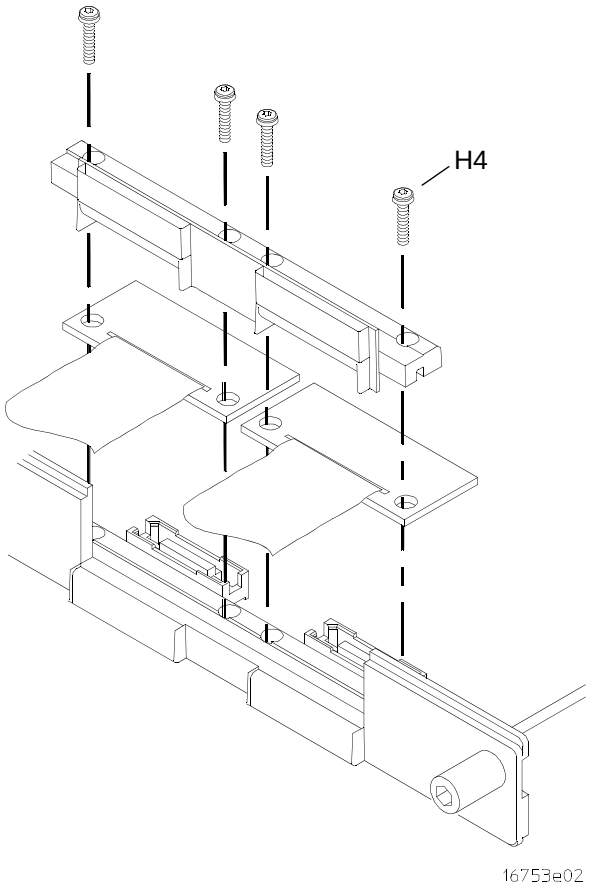
Instructions for removing or installing the module into the mainframe can be found in the installation guide for the mainframe.

If you don't have the installation guide for your mainframe, you can find the latest version on the Internet at www.agilent.com.

For example: to find the installation guide for a 16900-series mainframe, go to www.agilent.com and enter "16902B" in the quick search box. In the product page's Technical Support area, select "Manuals & Guides" to find the *16900-Series Logic Analysis System Installation Guide*.

To remove the logic analyzer cable

1 Remove power from the instrument
   a In the session manager, select Shutdown.
   b At the query, select Power Down.
   c When the "OK to power down" message appears, turn the instrument off.
   d Disconnect the power cord.
2 Remove the logic analyzer cable clamp.
   a Remove four screws that secure the logic analyzer cable clamp to the outside rear panel.
   b Remove the cable clamp from the rear panel.



3 Remove the logic analyzer cable.

   a Gently lift the logic analyzer cable end connector from the circuit board connector (J1, J2, J3, or J4).

4 If the logic analyzer cable is faulty, replace the cable and follow the next procedure to install the replacement logic analyzer cable.

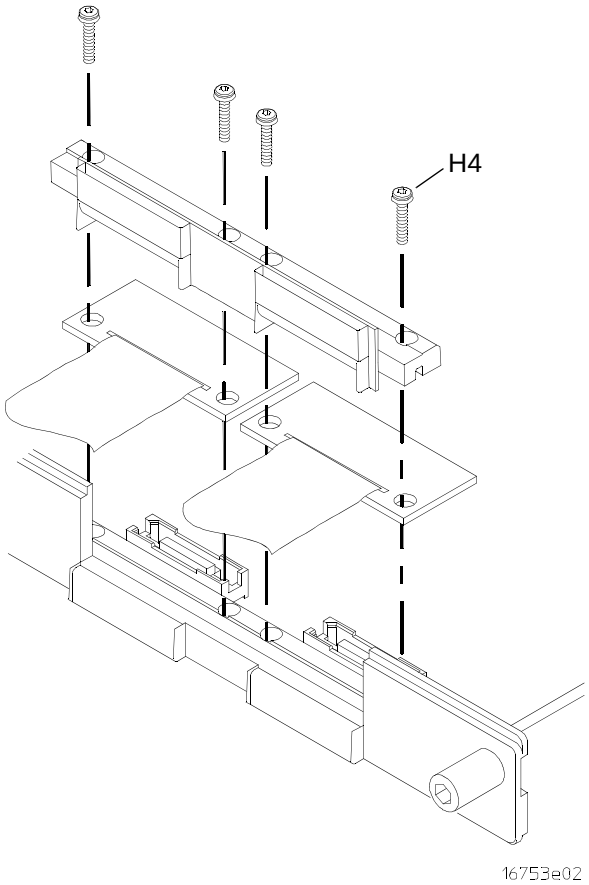
To install the logic analyzer cable

1 Connect the logic analyzer cable to the logic analyzer circuit board.

   a Insert the logic analyzer cable to the logic analyzer circuit board.

   b Align the logic analyzer cable end connector with the circuit board cable connector (J1, J2, J3, or J4) and gently apply pressure to seat the logic analyzer cable onto the circuit board connector.

   c Insert the top and bottom logic analyzer cable clamps into the rear panel.



2 Secure the cable clamp to the rear panel.

   a Install the four screws (H5) vertically through the cable clamp into both the cable clamp and the circuit board.

   b Tighten the cable clamp screws (H5) to 5 in/lb.

CAUTION If you over tighten the screws, the threaded inserts on the rear panel, the threaded inserts on the circuit board, or the cable clamp itself might break. Tighten the screws only enough to hold the cable in place, approximately 5 in/lb.

To replace the circuit board

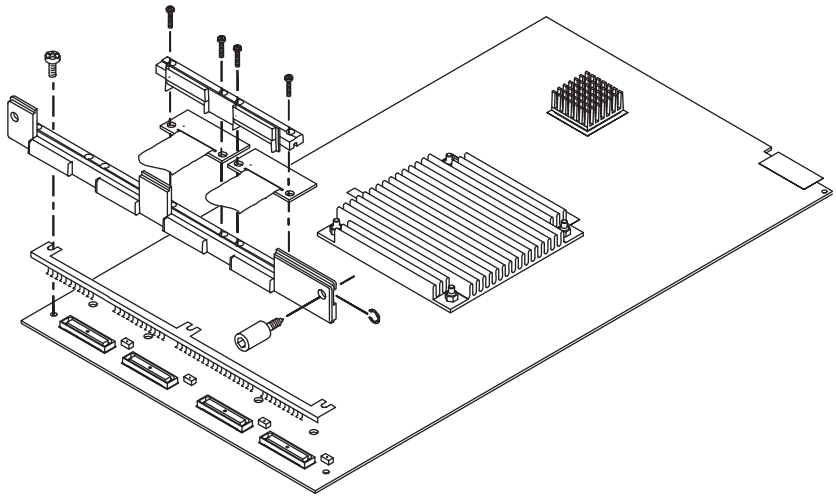
1 Remove the logic analyzer cables using the "To remove the logic analyzer cable" procedure on page 82.

2 Remove the four screws attaching the ground spring and back panel to the circuit board, then remove the back panel and the ground spring.

3 Replace the faulty circuit board with a new circuit board.

4 Position the ground spring and back panel on the back edge of the replacement circuit board. Install four screws to connect the back panel and ground spring to the circuit board.

5 Install the logic analyzer cables using the procedure "To install the logic analyzer cable" on page 84.



To return assemblies

Before shipping the module to Agilent Technologies, contact your nearest Agilent Technologies Sales Office for additional details. Information on contacting Agilent can be found at www.agilent.com.

1 Write the following information on a tag and attach it to the module.

- Name and address of owner.
- Model number.
- Serial number.
- Description of service required or failure indications.

2 Remove accessories from the module.

Only return accessories to Agilent Technologies if they are associated with the failure symptoms.

3 Package the module.

You can use either the original shipping containers, or order materials from an Agilent Technologies sales office.

CAUTION For protection against electrostatic discharge (ESD), package the module in ESD-safe material.

4 Seal the shipping container securely, and mark it FRAGILE.

7 Replaceable Parts

This chapter contains information for identifying and ordering replaceable parts for your module.

Replaceable Parts Ordering

Parts listed

To order a part on the list of replaceable parts, quote the Agilent Technologies part number, indicate the quantity desired, and address the order to the nearest Agilent Technologies Sales Office.

Parts not listed

To order a part not on the list of replaceable parts, include the model number and serial number of the module, a description of the part (including its function), and the number of parts required. Address the order to your nearest Agilent Technologies Sales Office.

Direct mail order system

To order using the direct mail order system, contact your nearest Agilent Technologies Sales Office.

Within the USA, Agilent Technologies can supply parts through a direct mail order system. The advantages to the system are direct ordering and shipment from the Agilent Technologies Part Center in Mountain View, California. There is no maximum or minimum on any mail order. (There is a minimum amount for parts ordered through a local Agilent Technologies Sales Office when the orders require billing and invoicing.) Transportation costs are prepaid (there is a small handling charge for each order) and no invoices.

In order for Agilent Technologies to provide these advantages, a check or money order must accompany each order. Mail order forms and specific ordering information are available through your local Agilent Technologies Sales Office. To locate a sales or service office near you, go to www.agilent.com/find/contactus.

Exchange assemblies

Some assemblies are part of an exchange program with Agilent Technologies.

The exchange program allows you to exchange a faulty assembly with one that has been repaired and performance verified by Agilent Technologies.

After you receive the exchange assembly, return the defective assembly to Agilent Technologies. A United States customer has 30 days to return the defective assembly. If you do not return the defective assembly within the 30 days, Agilent Technologies will charge you an additional amount. This amount is the difference in price between a new assembly and that of the exchange assembly. For orders not originating in the United States, contact your nearest Agilent Technologies Sales Office for information.

See Also "To return assemblies" on page 86.

Replaceable Parts List

The replaceable parts list is organized by reference designation and shows exchange assemblies, electrical assemblies, then other parts.

Information included for each part on the list consists of the following:

- Reference designator (if applicable).
- Agilent Technologies part number.
- Total quantity included with the module (Qty).
- Description of the part.

Reference designators used in the parts list are as follows:

- A Assembly.
- H Hardware.
- J Connector.
- MP Mechanical Part.
- W Cable.

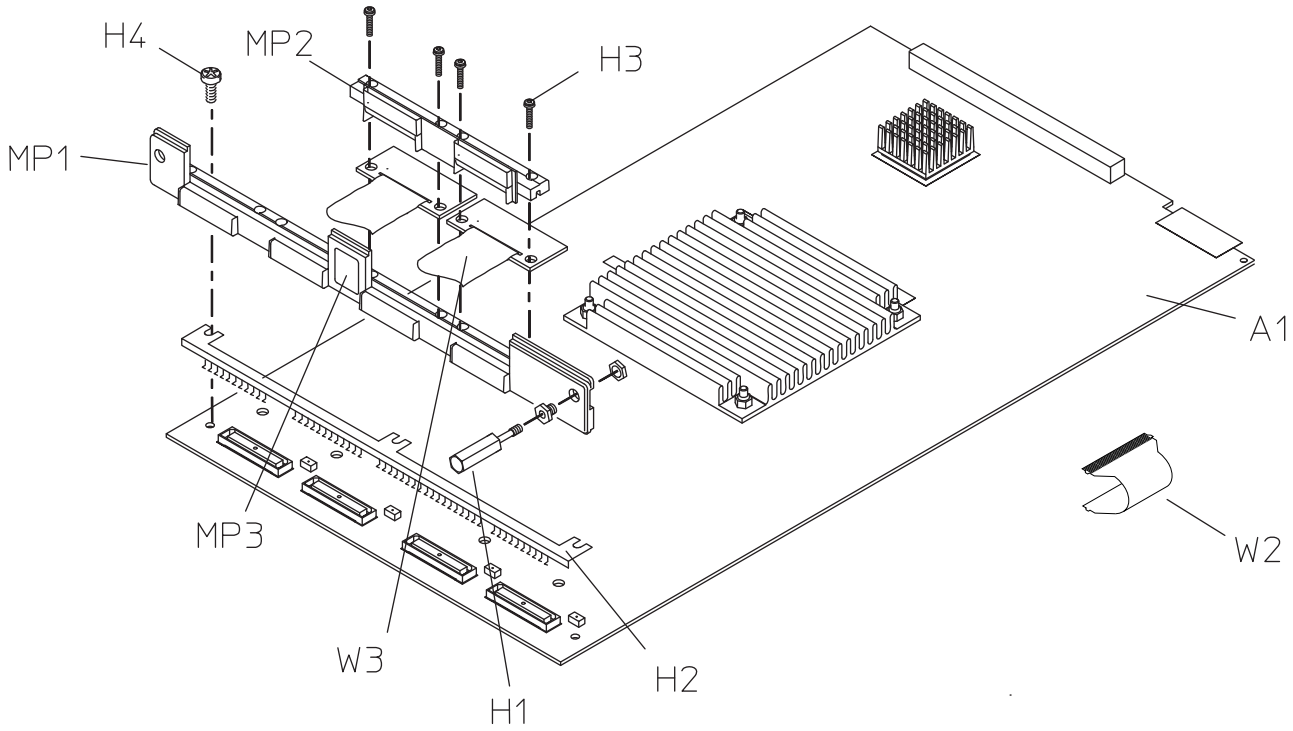


Figure 3 Exploded view of the 16962A logic analyzer

Table 11 Replaceable Parts, Exchange and Replacement Assemblies

Ref. Des.	Agilent Part Number	QTY	Description
Exchange Assemblies			
	16962-69501		Exchange Acquisition Board Assembly for 16962A
Replacement Assemblies			
A1	16962-66501	1	Acquisition Board Assembly for 16962A
	16760-60001	0	Stimulus Board Assembly (for cable test; see page 71)
H1	16900-62401 16900-62402	2 2	Captive Screw - Module Sleeve - Module
H2	16754-29101	1	Ground Spring
H3	0515-0375	8	M3.0x0.5 16mm T10 (Cable Clamp to Acquisition Board)
H4	0515-0430	3	MSPH M3.0x0.50 6mm T10 (Rear Panel to Acquisition Board)
H5	2950-0078	2	Nut, Hex, Double Chamfer, 10-32-THD, 0.067-IN-THK
	01650-94312	1	Label - Probe and Cable (on 90-pin connector)
MP1	16754-44101	1	Rear Panel
MP2	16754-41201	2	Logic Analyzer Cable Clamp
MP3	16962-94301	1	ID Label
W2	16960-60001	1	Flex Assembly Kit (2 pieces)
W3	16962-61601	4	Logic Analyzer Cable

For replaceable parts information for probing accessories, see the *Probing Solutions for Logic Analyzers Catalog*, literature part number 5968-4632E, available on Agilent's web site (www.agilent.com).

7 Replaceable Parts

8 Theory of Operation

This chapter presents the theory of operation for the logic analyzer card.

The information in this chapter is to help you understand how the logic analyzer operates. This information is not intended for component-level repair.

Block-Level Theory

The block diagram of the 16962A logic analyzer is shown below.

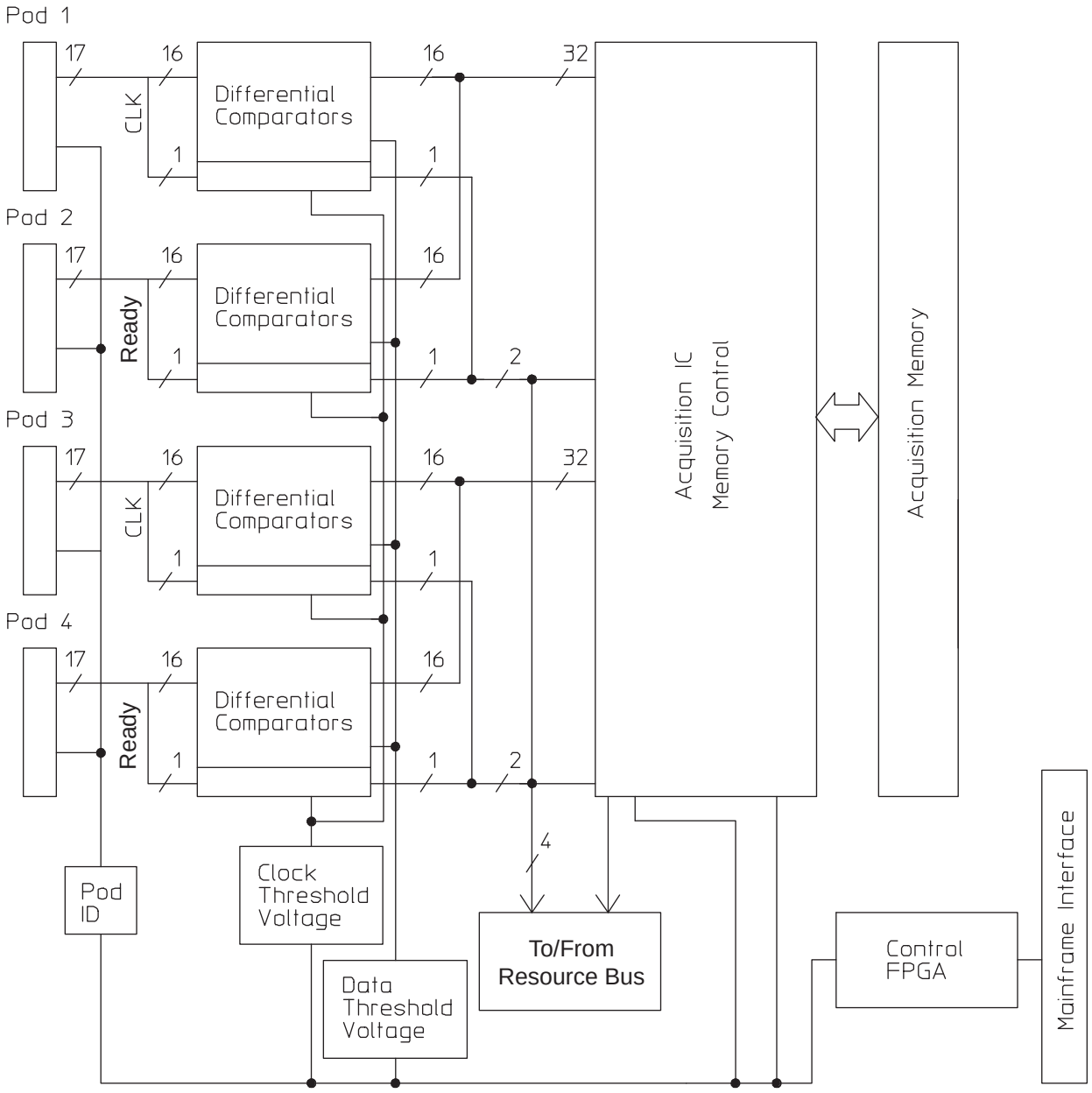


Figure 4 The 16962A logic analyzer

Probes

The 16962A logic analyzer card contains 4 probe pods. Each pod is comprised of two cables and contains 16 differential data channels, a differential clock channel, a user supplied threshold voltage, two serial I2C programming lines for configuring analysis probes, +5 V for powering analysis probes, a probe identification line, and 50 ground signals. Each cable has a 90-pin probe cable connector.

The pods provide +5 Vdc ±5% auxiliary power to each 90-pin probe cable connector. Each connector can deliver up to 300 mA with a maximum of 1.0 A total from the analyzer card. A current limiting circuit protects the +5 V cable power from current overload. The VCC_Enable signal is used to control power to an analysis probe. This allows analysis probes to be connected without powering down the analyzer and yet insures a clean +5 Vdc ramp to the analysis probe when power is applied by software.

A variety of differential and single-ended probes can be connected to the logic analyzer cables. Each probe type is uniquely identified by a different resistor value connected between its probe ID signal and ground.

Comparators

The comparators are differential input/differential output devices that interpret incoming data and clock signals as either high or low. A threshold voltage provided by an internal digital-to-analog-converter (DAC) is coupled to the negative side of the differential signal through a precision resistor. Alternatively, this voltage can be provided to the data channels by a user supplied threshold line in the probe cables. There are separate internal DAC driven thresholds for the data and clock in each pod.

In order to achieve performance, an extensive calibration is performed on each comparator when the board is manufactured and the results of this calibration are stored as Calibration Constants in non-volatile memory on the logic analyzer board. These constants are loaded into the comparators at power on.

Acquisition and Memory Controller IC

The Acquisition IC processes 64 channels of data and 4 channels of clock information. The Acquisition IC performs data sampling, sequencing, store qualification, pattern

recognition, and counting functions. State or Timing sample clocks are sent between cards in a multi-card module. Sampled data is decelerated and passed to a Memory Controller for storage in the Acquisition Memory RAM array.

The Acquisition IC also contains memory.

The Memory Controller stores data from the Acquisition ICs into the Acquisition Memory. It also unloads data from the memory array after an acquisition is complete, and it delivers the data to the mainframe display system through the mainframe interface connector. In addition, it can perform a search of stored data.

Acquisition Memory

The Acquisition Memory array is composed of DDR2 SDRAMs.

Resource Bus Connectors

Connectors J10, J11, J12, and J13 route state clocks, calibration signals, data search signals, control signals, pattern recognition signals, and control clocks between all cards in a multi-card module.

Mainframe Interface and Control FPGA

The Mainframe interface consists of an FPGA and the Mainframe Interface Connector. The connector brings power onto the card and provides for control of the card by the analyzer mainframe. It also provides a path for unloading acquired data to the analyzer display.

The FPGA converts bus signals generated by the mainframe processor into control signals for the logic analyzer card. It also provides centralized functions for the card such as I2C, Calibration signals, Flag routing, and Timing mode sample clock.

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